A NEW VME TIMING MODULE: TG8

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Abstract

The two accelerator divisions of CERN, namely PS and SL, are defining a new common control system based on PC, VME and Workstations. This has provided an opportunity to review both central timing systems and to come up with common solutions. The result was, amongst others, the design of a unique timing module, called TG8.

The TG8 is a multipurpose VME module, which receives messages distributed over a timing network. These messages include timing information, clock plus calendar and telegrams instructing the CERN accelerators on the characteristics of the next beam to be produced.

The TG8 compares incoming messages with up to 256 programmed actions. An action consists of two parts, a trigger which matches an incoming message and what to do when the match occurs. The latter part may optionally create an output pulse on one of the eight output channels and/or a bus interrupt, both with programmable delay and telegram conditioning.

I. INTRODUCTION

Until the advent of the Large Electron Positron (LEP) collider each new accelerator built at CERN had its dedicated timing system. Each system was tailored to the specific needs of the machine and integrated into the control system. As the working life of a large accelerator spans several decades, it becomes necessary after a certain period to update the control and timing systems. Such an upgrade was applied to the SPS timing system in 1985 [1] and subsequently it was decided to adopt the same system for LEP.

The rejuvenation of the PS control system is presently being implemented [2]. The TG8 timing module, described in this paper, will form an integral part of the joint PS/SPS/LEP timing system. The TG8 is based on a similar but simpler module, the TG3, currently in use at the SPS and LEP.

II. ACCELERATOR TIMING SYSTEMS

The typical real time response of a large accelerator control system is in the region of 10 to >1000ms. Whilst this is adequate for many applications there always remains the requirement to activate equipment with a finer real time resolution. Such an application would be the ramping of the main power converters around LEP. This is achieved by using a separate timing system.

General Machine Timing (GMT) systems for large accelerators normally consist of three parts:

- a central timing generator
- a distribution network
- receiving modules

This article concentrates on the VME receiving modules, although the other two points are also discussed.

The central timing generator is constructed on a single IBM/PC compatible card and is referred to as the Master Timing Generator (MTG). It is basically a large memory which is pre-loaded with machine related timing information for each cycle. At specific times the MTG broadcasts this information over the distribution system. The MTGs for each machine are synchronized to a CERN wide 1ms reference clock.

For the SPS and LEP machines it was decided to use Time Division Multiplex (TDM) techniques, conforming to CCITT Recommendations, to form a backbone for the distribution network. This was adopted due to the long distances involved and also to reduce the number of cables required in the two tunnels. Because of its much smaller size the PS will retain the use of dedicated cables. The overall timing transmission standards used at CERN have been described elsewhere [3].

The receiver modules (TG8s), so named because they have eight output channels, are connected to the timing network and receive information in the form of frames referred to as events. The use and operation of the TG8 is described in more detail later.

III. EVENTS

A. Standard events

Standard events mark precise times within a machine cycle, i.e transition, start fast extraction, end of flat top etc. In particular, they are used to initiate actions in the TG8 action table. Such an event has a "header", identifying it with a given machine, plus a one byte code specifying which standard event it is. In addition to this, each standard event is also tagged by a cycle type, and the occurrence number of that type in the super cycle, namely the Cycle Number.

B. 1kHz Clock Events

The 1kHz event is used to synchronize up to seven preceding events which may have arrived during the previous millisecond period. This type of timing frame is thus

specially treated by the TG8 hardware, and in addition to its synchronization usage, it may also be used to clock any of the eight TG8 counters. Like any other event, the 1kHz events can be used to trigger TG8 actions.

C. Date and Time of Day Events

The MTGs receive the Central European Time information each second via a 77.5kHz radio signal originating from a 50 kW transmitter located at Mainflingen, Germany. They receive this information in the form of an ASCII string and subsequently convert the data into eight bytes containing the BCD values for second, minute, hour, day, month and year. The MTG broadcasts these events precisely over the network each second. They have lower priority than the other events so that if a clash occurs then for example, the year or month events will be transmitted during the next millisecond time slot.

In addition, a time event is generated containing the second, minute and hour information and also a date event comprising of the day, month and year. These two events can be used to trigger actions at specific calendar or date times.

D. Telegrams

The telegram message is composed of a set of numbered parameters which describe the particle beam, currently being produced by a group of machines. For historic reasons, these parameters are referred to as groups, a term arising from the way the telegram used to be distributed as a serial bit stream. Each parameter is described by two quantities, namely; the group number, and the corresponding group value. The group number determines which parameter is selected, and the group value specifies a signed sixteen bit value belonging to the selected parameter [4]. Telegrams are associated with a machine, or group of machines, in the same way that standard events are. The telegram message however, do not trigger an action, rather they are used to condition whether or not an action starts executing in the first place.

IV. TIMING FRAMES

The network distributes information as a sequence of four byte frames; up to eight of these timing frames can occur each millisecond. The present SPS/LEP timing system generates four frames per millisecond which has so far proved to be adequate. A timing frame has an identifying header byte, which classifies what kind of information it is (telegram, event, time of day etc.) followed by three bytes which further specify the frame within the header class. The timing frames are transmitted during the one millisecond time slots and are validated at the end of this time. Thus the resolution of a frame, and hence any timing event on the network is one millisecond.

The timing slot boundaries are in fact marked by the 1kHz clock frames, leaving seven time divisions in which other frames can be sent. Thus no more than seven timing events can occur per millisecond, as the eighth division is used by the millisecond clock.

V. SIGNAL STANDARDS

The original machine timing signal standard used at CERN was developed over 30 years ago. This "blocking oscillator" circuit generates a transformer isolated pulse with an amplitude of 24 volts and a duration of 1.5us. It was designed specifically to transmit timing pulses over 50 Ohm co-axial cables in hostile and noisy environments. It is still in use throughout the PS and also in the original SPS control system.

However, for the SPS upgrade and also for LEP, it was decided to adopt commercial standards rather than continue with an in-house system. The standard chosen conforms to the electrical characteristics defined by CCITT Recommendations V.11 and X.27 and EIA specification RS-485. Each frame is Manchester encoded and the local line drivers are transformer isolated at the driving end. The data format adopted is supported by integrated circuits from National Semiconductor (the NS8342/8343 transmitter/receiver set).

VI. TG8 HARDWARE

A. Overview

The TG8 is a timing module conforming to the VME standard. It operates in the slave mode and also as an interrupt generator. The TG8 VME timing module consists of two sections: a receiver part and a process part. The basic purpose of the receiver part is to accept all the frames from the timing network and to pass on the treated events to the process part. The process part compares each received event with a set of pre-loaded parameters contained in a portion of the on-board memory referred to as the "action table". These parameters are a subset of the total events contained in the MTG's memory.

If a valid comparison is found between the received event and the parameters loaded in the "action table", then that specified action is performed. This will normally result in interrupting the VME crate's CPU, and/or generating a TTL level pulse on one of the module's eight front panel outputs. The options are user programmable.

B. The Receiver Part

In the MTG, the NS8342 integrated circuit frames the 32 bit events into four bytes. Each frame is enveloped within a predefined start/end sequence and in addition each byte starts with a synchronizing bit and ends with a parity bit. The TG8's NS8343 receiver chip performs the reverse operation and reconverts the frame to a 32 bit NRZ word. In addition, the NS8343 contains a seven bit error register which indicates, amongst other things, the detection of a mid-bit transition fault, an invalid ending sequence and also a parity error.

The contents of this register are used by the TG8 for error detection.

The receiver continuously monitors the reception of the 1ms clock events. If a clock is missing then the hardware generates a substitute clock, produces a 1ms "watch-dog" error and informs the process part of the error situation. All of these error bits can be read via the VME bus.

The interface between the NS8343 integrated circuit and the process part incorporates a XILINX 3030 gate array. It contains all the logic necessary to perform the above functions.

C. Process Part

The core of the process part is the Motorola MC68332 integrated circuit. This chip is a powerful microcontroller based on the MC68020 microprocessor. It contains the various functions required for embedded control applications such as 16 bit timers, RAM, UART, along with digital input and output facilities. A second XILINX is used, this time a 4008 containing 8000 gates, which contains all the logic to control the counters and interrupt circuits for each of the eight outputs.

The module uses 16 bit VME data transfers and 24 bit address decoding. In order to optimize communications between the VME bus and the timing card, two kbytes of the TG8's total memory are dual ported. These two kbytes can be accessed both from the VME bus and the MC68332 microcontroller. For system configuration reasons, this dual port memory can be placed on any location in the 16Mbyte VME memory map. The module also contains 1Mbit of EPROM, used to contain the microcontroller's firmware, plus 512 bits of static RAM along with a 256*48 bit Content Addressable Memory (CAM) which contain various user tables.

The firmware's main task is to treat interrupts generated by the receiver part. For every valid frame received the MC68332 uses the speed of the CAM to compare each event with up to 256 pre-loaded trigger conditions. If a valid comparison is detected then the microcontroller, using the XILINX gate array, loads the specified counter with the appropriate delay, selects the clock unit and prepares the hardware to generate an output pulse and/or a VME interrupt when the selected counter has been decremented to zero.

D. The Action Table

The action table is partitioned into two sections referred to as the trigger part and the action part. The trigger part is located in the CAM, whilst the action part is located within the RAM.

The trigger part contains the full 32 bits required for the event definition, plus the 16 bit PLS identifier. The action part describes what the TG8 must do when triggered, such as setting up a counter to make an output pulse etc. With the exception of the first byte header, "don't care" values (Hex.FF) can be placed in any of the other three byte fields. In this case they will always match with the corresponding field of the event being processed, no matter what it contains. Thus up to three "don't care" wild cards can be used in order to specify a trigger condition.

VII. TG8 SOFTWARE

From a software point of view, the major task is the management of the action table. As previously mentioned, the table contains 256 rows each of which describes a unit of work to be carried out by a TG8. Each row is composed of a trigger and an action to be performed when the trigger conditions occur. A TG8 unit of work is specified by:

1) The trigger condition, which is composed of an event specification and an optional telegram condition. Both of these must occur before the rest of the action table row is processed.

2) The delay, which consists of a clocking train selection, and the number of ticks to be counted in the specified train.

3) The mode, which describes how the TG8 counters may be combined to produce counter chains, in which the output of one counter triggers the start of another; or burst mode, in which pairs of counters are combined to produce a burst of pulses.

4) The result part, which will be either a VME bus interrupt, or an output pulse, or both. If a bus interrupt is specified, then a user specified callback routine will be invoked. A library for the VME chassis processor will be provided.

Each TG8 module in a given VME crate is controlled by a device stub controller (DSC) processor [5], which runs a diskless real time POSIX-4 compliant version of Unix supporting all the usual features such as NFS, TCPIP, X-Window client etc. Applications running at this level use the TG8 library to control the TG8 modules resident in the same VME crate, and are able to communicate with Unix based work stations running X-windows and OSF Motif.

The application program interface (API) will consist of a C language binding to a TG8 library in which functions manipulate structures containing action table rows. Care must be taken when combining these rows into an action table for a particular TG8. Checks must be carried out to ensure that the individual rows do not compete for TG8 resources, such as counters, in real time. Some simple checks can be performed which ensure a basic level of consistency, but full checking would depend on knowing how the trigger conditions will actually occur in real time, which is clearly impossible.

VIII. CONCLUSIONS

The consolidation of CERNs different machine timing systems has been proposed and discussed many times during the past two decades, without significant results. This present proposal was initially outlined at a joint PS/SL Control Users

Forum held in Chamonix, France, during April 1990. In June 1991 the PS and SL control groups agreed on a specification for a common machine timing system [6]. This entailed using the IBM/PC based Master Timing Generator, as presently used in the SL division and to produce a new VME timing module compatible with both timing systems.

Presently, the prototype TG8 module is being tested in the laboratory using the SL timing system. It is planned to test the unit with the PS system in the first quarter of 1992. It is therefore too early to arrive at any definite conclusions, particularly regarding costs. The price of the "state of the art hi-tech" components used in the TG8 is falling rapidly and clearly the production units will be far less expensive than the present prototype. On the cost basis however, one must consider at what stage in a systems lifetime is it cost effective to develop a completely new system rather than to develop complex new modules compatible with two different existing systems.

IX. ACKNOWLEDGEMENTS

Many people have contributed to the upgrading of the PS/SL control and timing systems, but particular mention must be made to the two group leaders, K.-H. Kissler and F. Perriollat, who have stoically pursued the project. Also to P. Nouchi and R. Parker for their invaluable contributions.

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