Fermi National Accelerator Laboratory

FERMILAB-TM-1895

A High Speed, Wide Dynamic Range Digitizer Circuit for Photomultiplier Tubes

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June 1994

Operated by Universities Research Association Inc. under Contract No. DE-AC02-76CHO3000 with the United States Department of Energy

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A circuit has been designed for digitizing PMT signals over a wide dynamic range (17-18 bits) with 8 bits of resolution at rates up to 53 MHz. Output from the circuit is in a floating point format with a 4 bit exponent and an 8 bit mantissa. The heart of the circuit is a full custom integrated circuit called the QIE (Charge Integrator and Encoder). The design of the QIE and associated circuitry reported here permits operation over a 17 bit dynamic range. Tests of the circuit with a PMT input and a pulsed laser have provided respectable results with little off line correction. Performance of the circuit for demanding applications can be significantly enhanced with additional off line correction. Circuit design, packaging issues, and test results of a multirange device are presented for the first time.

1. Introduction

High energy physics experiments running at high interaction rates frequently require long record lengths for determining a level 1 trigger. The easiest way to provide a long event record is by digital means. In applications requiring wide dynamic range, however, digitization of an analog signal to obtain the digital record has been impossible due to the lack of high speed, wide range FADCs. One such application is the readout of thousands of photomultiplier tubes in fixed target or colliding beam experiment calorimeters.

A custom integrated circuit called the QIE along with a small circuit board has been designed to meet this difficult digitization requirement. The circuit is small enough to be located immediately behind a dense array of PMTs with PMT diameters as small as 19 mm. Eventually it is expected that the complete digitization circuit could be attached directly to the base of a PMT. Thus the signals leaving the PMT base would be digital, less susceptible to noise degradation, and easily stored for a level 1 trigger.

First measurements of a QIE chip operating on a low range have shown the effectiveness of the QIE approach in a test beam at BNL. Noise floor levels of 2 fC were measured in a noisy beam environment with the circuit running at 53 MHz [1]. Since the first results were reported, a wide range QIE and miniaturized circuits have been built and tested.

*Work supported by the U. S. Dept. of Energy under contract No. DE-AC02-76CHO3000.

2. General Operating Principles

The digitization circuit uses a custom ASIC along with a commercial FADC to digitize charge (current) input signals. A very simplified block diagram of the circuit is shown in Figure 1. The custom integrated circuit simultaneously performs two functions: 1) The QIE integrates binary weighted divisions of the input signal for a period of time, identifies the range of the input signal, and presents that information at the QIE output in digital form as a 4 bit exponent. 2) At the same time, the QIE

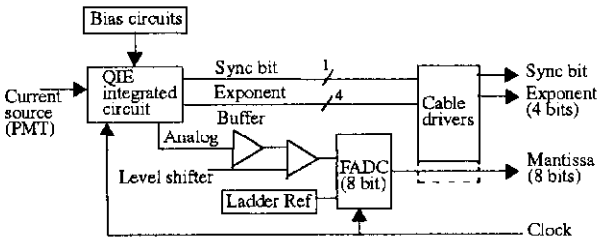

Figure 1 - Digitizer Circuit Block Diagram

selects the integrated signal in the range of interest and presents it to the QIE analog output for digitization. After buffering and level shifting, the analog signal is applied to an 8 bit FADC. The output of the FADC is the mantissa of a floating point number that represents the charge delivered to the QIE in a sampling period. A synchronization bit is generated by the QIE for timing purposes. Both the sync bit and the exponent bits from the QIE have separate output driver

circuits. (In later versions of the board, the QIE outputs and the FADC outputs will share a common custom driver chip as indicated by the dashed line.)

A grasp of the operating principles of the QIE chip is helpful for understanding the performance of the digitizer circuit. Detailed descriptions of the QIE architecture have been described previously [1], [2]. However, a brief review is appropriate to better understand the test results.

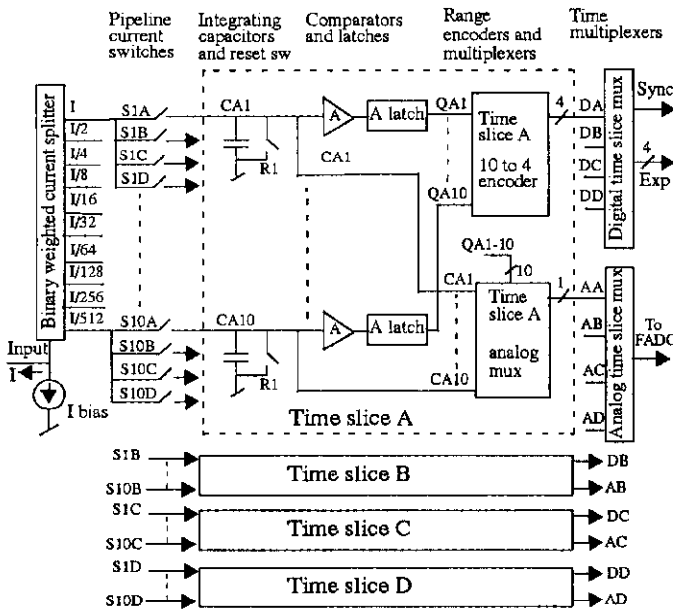

Figure 2 - Simplified block diagram of QIE ASIC

The QIE device processes information in 4 steps as a 4 stage pipeline. One data sample through the chip can be followed by referring to the binary weighted current splitter and Time Slice A blocks in Figure 2. The input signal received from a current source such as a PMT is added to a small bias current and the sum of these signals is applied to a binary weighted current divider. During the first clock cycle, the outputs from the binary weighted current splitter are applied though pipeline current switches S1A-S10A to a set of 1 pF capacitors where charge is integrated for a period of time (e.g. 19 ns). The voltage integrated on the array of capacitors is applied to a set of comparators. During the second clock cycle, the comparator outputs are allowed to settle and the comparator outputs are latched. The nature of the binary weighted current divider means that the outputs of the comparators form a 10 bit digital thermometer code of 1s and 0s. The transition between comparator 1s and 0s is a measure of the input signal amplitude range. During the third clock cycle, the comparator outputs are encoded into a 4 bit number representing that range. The digital number is presented at the output of the QIE as the exponent of a floating point number. The outputs of the comparators are also used to control an analog mux which selects the correct integrated capacitor voltage (i.e. QIE range) for digitization off chip. During the third clock cycle, the analog mux output signal has time to settle before digitization. During the fourth clock cycle, the integrating capacitors in time slice A are simultaneously reset by switches R1. Processing of the next three data samples is handled by other pipeline current switches and the blocks labeled Time Slice B, C, and D in Figure 2. Additional digital and analog multiplexers are used to select the appropriate time slice information for readout. Due to the pipeline nature of the QIE, digital and analog information for a particular integration period is output from the QIE chip approximately two clock cycles after it occurs. A synchronization pulse is generated with the output information to identify the time slice which is transmitted.

Figure 3 is a photograph of the QIE die which was used on the test boards described in this paper. The die, which measures 4.5 x 4.5 mm, is expected to be smaller in future submissions. The binary weighted current splitter is located near the bottom of the die and the processing circuitry for the four time slices can be seen in the center of the die.

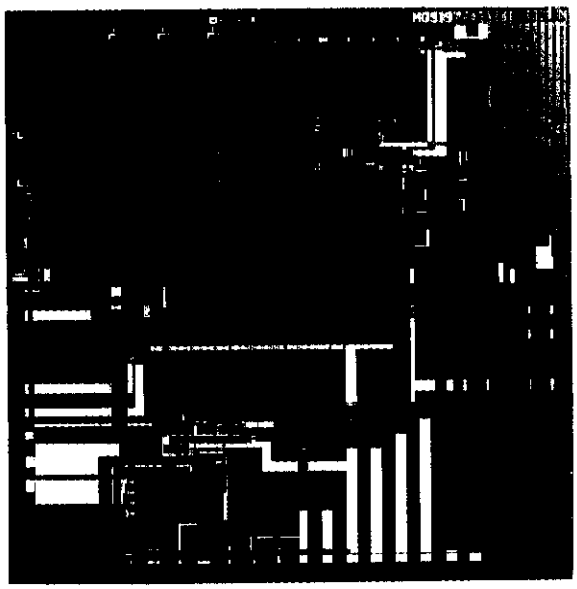

Figure 3 - QIE die photograph

Figure 4 shows the QIE analog and digital outputs for a 10 range QIE chip. Also shown are the digital codes for the associated 8 bit FADC. As the integrated input signal increases from 0 pC to 1023 pC, the QIE analog mux changes ranges starting at the I range and proceeding to the I/512 range for the largest signals. For each range, an analog signal which has a value between -1 and -2 volts is presented at the QIE analog output for digitization by a FADC. (To avoid problems associated with comparator offset variation which affects the range switch points, the FADC range is set to be slightly wider than the output range of the QIE.) Small variations in gain and offset for each range are expected to be corrected in software. On the I range (most sensitive range), the exponent output is 0000 and the analog signal to the FADC increases from -1 to -2 volts as the input charge increases from 0 to 1 pC. For signals slightly larger than 1 pC, the I/2 range comparator flips causing the encoded 4 bit exponent to become 1000, while at the same time the output analog signal level returns to -1 volt. The

cycle repeats itself for each range with the digital exponent information presented in Gray Code form. The horizontal

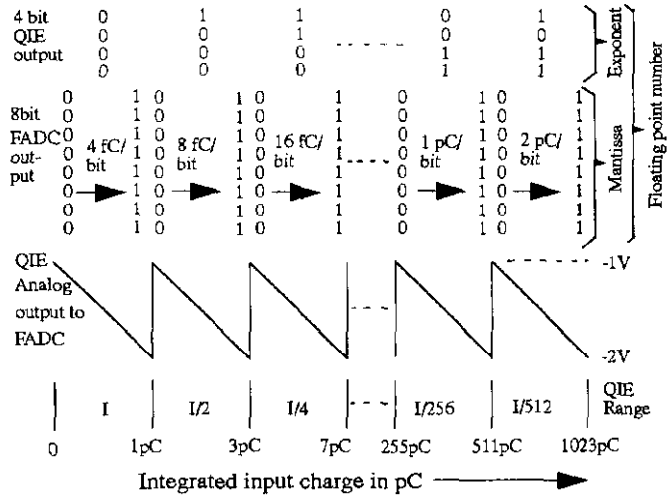

Figure 4 - Analog and digital output versus input charge

scale in Figure 4 is not linear for illustrative purposes. The QIE response along with the external FADC provides a close approximation to a logarithmic FADC which is well suited to measurements of PMT outputs. By comparing the charge resolution and the charge ranges shown in Figure 4, it is seen that the measurement resolution improves as the signal size increases. On the highest range, the measurement resolution is between 1 part in 256 and 1 part in 512.

3. PMT Digitizer Circuit Board

Several different circuit boards have been designed for the digitizer circuit. All of the boards are intended to fit behind a dense array of PMTs. The circuit boards are typically 2.3 cm x 15 cm. Input to the board is through a short (5 to 15 cm) coax cable and output is through a ribbon cable which also provides power to the board. To save space, the QIE and FADC are wirebonded directly to the circuit board and encapsulated or covered. In Figure 5, the uncoated QIE and its bias circuitry are located on the right hand side, while the uncoated FADC is left of center. Currently the Analog Devices AD9002 FADC is

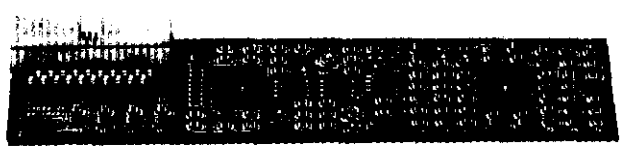

Figure 5 - PMT digitizer circuit board with QIE and FADC

being used. Discrete buffer amplifiers and a level shifter are located between the two devices. Fusing and the relatively large I/O connector are located on the far left. In future devices, much of the biasing circuitry around the QIE will be incorporated into the QIE along with some of the buffer amplifier circuitry.

The QIE and FADC each dissipate several hundred milliwatts. To remove heat from these devices, thermal vias connect the die pads to relatively large copper pads on the back side of the board. A heat sink is mounted on the back side of the board for heat removal. A shield which is not shown is intended to cover the circuit board to reduce EMI.

4. Test Results

The results presented are for a 9 range QIE device (the I range was not active) operating with the 8 bit Analog Devices AD9002 FADC. Although the board has been run at 53 MHz, the tests reported here were run at 10 MHz. The purpose of the tests was to measure the offset and gain variations for each range and derive the overall linearity of the device, check the stability of the correction constants, measure the noise with a PMT input, and identify potential problems with operation at higher sampling rates.

The first tests performed used a 16 bit DAC controlled pulser and a shaper circuit to drive a voltage to current buffer which injected charge into the digitizer board. PMT photostatistic effects were not present since a PMT was not used. The test pulse had a 10 ns tail which fit well within the 100 nsec integration time. The peak current rating of the pulser circuit limited testing of the QIE to the I/2 through the I/64 ranges. Figure 6 shows FADC output counts and the different QIE ranges as a function of the 65000 amplitudes possible from the pulser using data from only one of the four time slices. The response shows from left to right the FADC digital output with the QIE on the I/2, I/4, I/8, I/16, I/32, and I/64 ranges. This view is similar to figure 4 but the horizontal

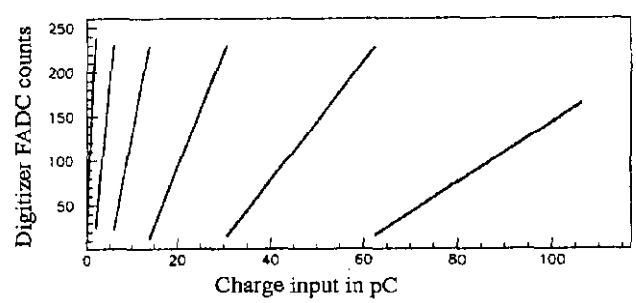

Figure 6 - Digitizer FADC output versus input charge

scale is now linear. It should be observed that the range switch points have slightly different FADC values but at no time does the signal fall outside the 8 bit FADC range. A major contribution to the switch point variations is differences in offset between the comparators which flip to change ranges. The gain between adjacent ranges should change by exactly a factor of two. Errors in this ratio were found to vary from 0.1 to 2.0%.

In addition to switch point variations that occur within a time slice, there are small variations which occur between time slices (sampling capacitors). One is pedestal variation which is defined as the variation in FADC counts between time slices for the bottom of the I/2 range (i. e. 0 input). Pedestal variation

is +/- 2 counts. The second is gain variation which shows up as differences in slope for each of the segments in Figure 6. This difference, which is due to slightly different integration capacitor values in each time slice, amounts to +/- 0.1 to 0.3%. Noise from the pulser circuit, which amounts to 3-4 counts (24-32 fC) on the I/2 range, is considerably higher than the noise floor of the digitizer circuit. Nevertheless, good low scale measurements were taken.

Intercept and gain correction constants from the segments in Figure 6 were derived and stored for later use. One week later the constants were used on a new single time slice data run to generate the highly linear composite (I/2 to I/64)

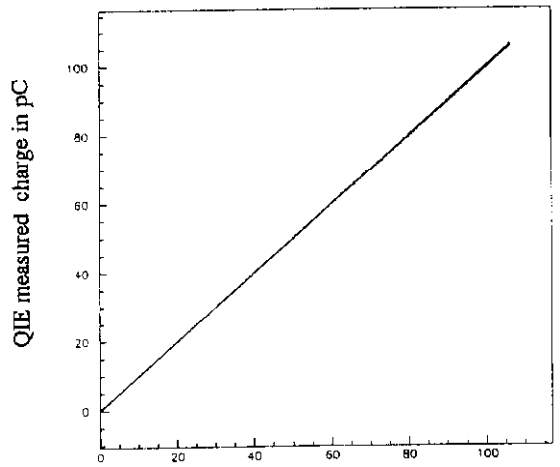

Figure 7 - Digitizer response corrected for gain and offset

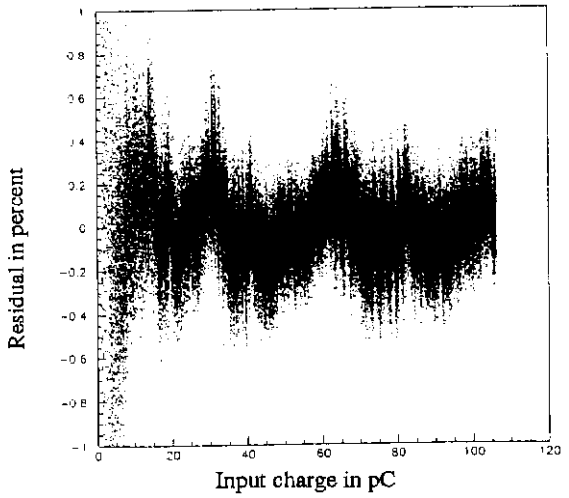

Figure 8 - Digitizer circuit residuals from a straight line

response shown in Figure 7. The residuals from a straight line shown in Figure 8 are due to LSB binning of the FADC, common board noise which affects all ranges in a similar manner, FADC nonlinearity, and charge injector noise. A common residual structure of +/- 0.2% is found on each of the 6 current range segments. This nonlinearity is probably due to the FADC and should be correctable (if necessary). A measure of the ultimate resolution of the digitizer circuit can be seen in Figure 9 which plots the fractional output rms as a function of

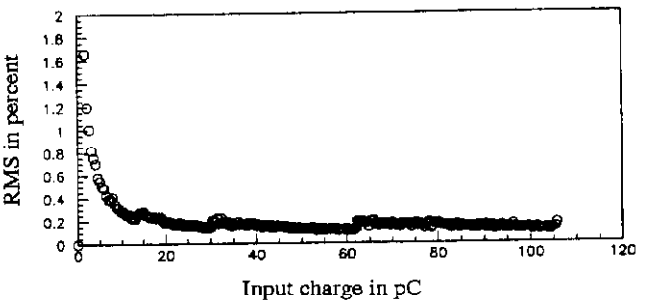

Figure 9 - Digitizer rms versus input charge

input charge. The higher rms at low input charge is simply due to the previously mentioned pulser circuit noise and is not present with a PMT input. At higher input levels, the rms is seen to vary smoothly between 0.1 and 0.2% as expected. It is particularly important to note that this level is substantially below the 0.7 to 1.0% detector resolution that can be expected with a high quality CsI scintillator and PMT. Also, it is particularly encouraging to note that calibration constants have been found to remain valid for relatively long periods of time, implying that frequent calibration is not necessary.

Another series of tests were run on the digitizer board using a small PMT (Hamamatsu R5330 6 Stage) and a pulsed laser as shown in Figure 10. These tests provide a more

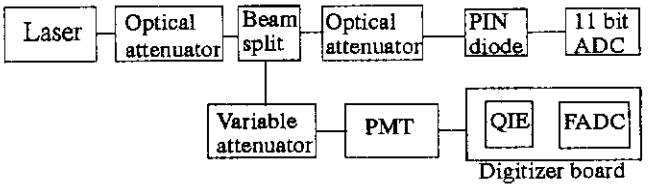

Figure 10 - Laser input digitizer test setup

realistic input for the digitizer circuit. A PIN photo diode and an 11 bit ADC were used to provide an input charge reference. The optical attenuator in front of the PMT was used to lower the input signal to the PMT for the I/2 to I/128 ranges. Use of the laser test setup allowed the digitizer to be tested over the full QIE range of I/2 to I/512. Since the digitizer circuit input comes directly from a PMT, the noise is lower than before. However, photostatistics are readily apparent on the lower ranges. Without unusual precautions for reducing external noise sources, the noise of the digitizer circuit was measured to be 2.4 fC rms (0.3 FADC counts) on the lowest range. A plot similar to Figure 6 was generated for all of the QIE ranges.

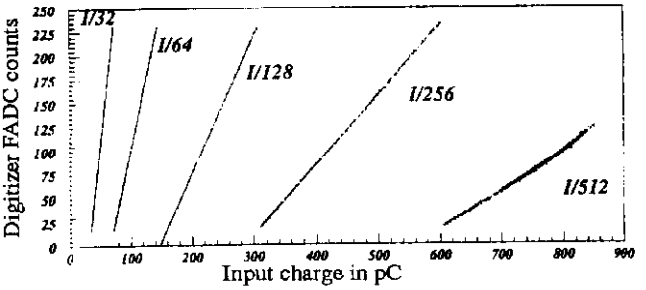

Figure 11 - Digitizer upper range response

Results on the lower ranges are very similar to Figure 6. The upper ranges which could not be measured with the current pulser are shown in Figure 11. The nonlinearity which appears on the I/512 range is believed to be in the PMT. With little off line correction, the laser data closely fits a straight line. Figure 12 shows the data from a test run assuming that all the gains vary by a factor of two and the same offset applies to all ranges (i.e. there are no individual range and offset corrections). Tests are continuing to evaluate the number of correction constants needed as a function of the accuracy required. At this time, it appears that offset and gain corrections for each of the 10 ranges should provide better than a 0.5% accuracy over the full dynamic range.

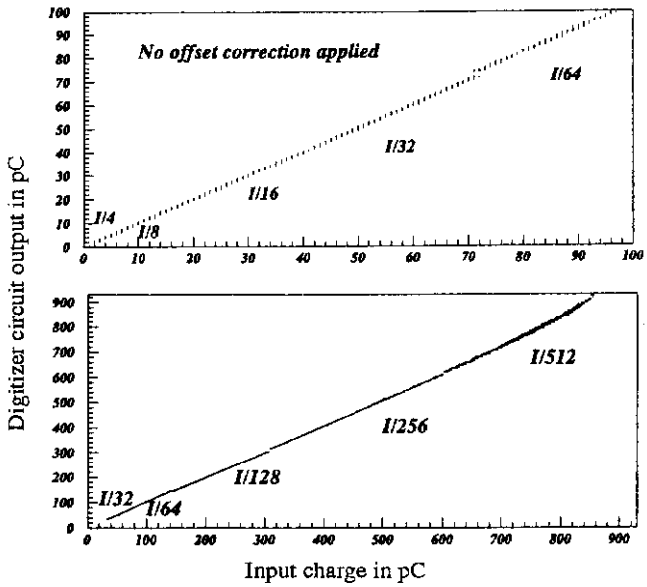

Figure 12-Digitizer response (without corrections applied)

The digitizer board has been run at 53 MHz. There were some minor problems such as slow buffer amplifier response and cable drive capability. These are not considered to be serious. However, operation at this higher frequency has shown a problem which is described as "charge loss". There is not a problem if a pulse lies entirely within one sampling interval as shown in Figure 13a or if all digitized samples use the same QIE range. In normal operation, the parasitic capacitance on each range is charged along with the integration capacitor. The parasitic capacitors are somewhat different on each of the ranges. If a switch occurs from a higher range to a lower range when a pulse straddles sample intervals as shown in Figure 13b, the charge on the parasitic of the higher range is not integrated on the sampling capacitor and is "lost". The magnitude of the problem depends on the waveshape being digitized and the sampling interval. For an experiment running at 53 MHz with pulses that have a 25 ns fall time, the error between some ranges could be as high as 5-10%. Work is in progress to characterize the charge loss issue and determine how much improvement can be obtained with off line correction.

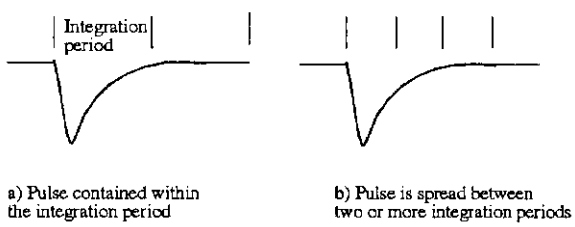

Figure 13 - Charge loss sampling condition

The issue of charge loss, however, is being addressed primarily by a new QIE design which reduces the magnitude of the problem and also performs on chip compensation. Simulations have shown the problem to be reduced by an order of magnitude. Chips with the new design have been received and testing has begun. The early QIE design could be used by some experiments while others may require a device in which the charge loss has been compensated.

5. Conclusion

A unique integrated circuit is being developed for fast digitization of charge (current) signals. The circuit is currently intended for photomultiplier tubes but other applications are possible. KTEV, a major fixed target experiment at Fermilab, has adopted the QIE ASIC to digitize signals from a large array of CsI crystals and PMTs. Preliminary test results have provided much encouragement. A 25 channel array is currently being instrumented with the digitizer circuit for a beam test in 1994.

6. Acknowledgments

Several individuals have made significant contributions to the QIE digitizer project. The authors would like to thank Sten Hansen of the Fermilab Physics Department for his engineering assistance with the QIE test boards. We would also like to thank Al Dyer of the Detector Electronic Systems Group for his laboratory assistance and Hogan Nguyen of the Fermilab Physics Department for his assistance with the YAG laser system.

7. References

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[2] R. J. Yarema, et. al., "A Fast, Wide Range Charge Integrator and Encoder ASIC for Photomultiplier Tubes", IEEE Trans. on Nuclear Science., Vol. 40, No. 4, August 1993, pp. 750-752.