Design and Commissioning of the APS Beam Charge and Current Monitor*

X. Wang, F. Lenkszus, and E. Rotela
Advanced Photon Source
Argonne National Laboratory
9700 S. Cass Ave.
Argonne, IL 60439

*Work supported by the U.S. Department of Energy, Office of Basic Energy Sciences, under Contract No. W-31-109-ENG-38.

Design and Commissioning of the APS Beam Charge and Current Monitors[1]

X. Wang, F. Lenkszus, and E. Rotela
Argonne National Laboratory, Argonne, Illinois 60439

Abstract

The non-intercepting charge and current monitors suitable for a wide range of beam parameters have been developed and installed in the Advanced Photon Source (APS) low energy transport lines, positron accumulator ring (PAR), and injector synchrotron. The positron or electron beam pulse in the APS has charge ranging from 100pC to 10nC with pulse width varying from 30ps to 30ns. The beam charge and current are measured with a current transformer and subsequent current monitoring electronics based on an ultrafast, high precision gated integrator. The signal processing electronics, data acquisition, and communication with the control system are managed by a VME-based system. This paper summarizes the hardware and software features of the systems. The results of recent operations are presented.

INTRODUCTION

Non-intercepting high accuracy beam current monitoring systems are required for the measurement of total charge, peak current, lifetime, and absolute beam loss. Figure 1 shows the layout of the charge and current monitors in the APS. All monitors shown in Fig. 1 have been installed and commissioned except those in the storage ring. The charge and current monitors described here feature new generation beam current transformers (1), a VME current monitoring electronics module based on an ultrafast, high precision gated integrator described in (2), graphical display and operator interface, and the current transformer housings with emphasis on noise shielding and grounding and use of standard commercial components.

DESIGN

A block diagram of the system and associated timing of a completed cycle are shown in Fig. 2 and Fig. 3, respectively.

The passage of a beam pulse through the current transformer induces a pulse siganl at the transformer's secondary winding. After suitable preamplification the signal is sent to the instrument room. The beam current monitoring electronics unit consists of a 6U VMEbus board that occupies a single slot in the card cage. The main features of the unit include a fast gated integrator with automatic baseline subtraction, completely programmable timing circuitry over the VMEbus, and an on-board 12-bit

---

[1] Work supported by U.S. Department of Energy, Office of Basic Energy Sciences, under contract no. W-31-109-ENG-38.

A/D converter. A beam pretrigger derived from the linac timing system enters a programmable delay generator that triggers a programmable width generator. This produces the pulses used to control the linear gate of the gated integrator. When the gate is opened by the gate pulse, the signal passes to the fast integrator. The integrator holds an output DC level proportional to the beam charge and current after the gate window is closed. This DC level is digitized by a 12-bit A/D converter linked to the VMEbus. A reset pulse returns the gated integrator's output to zero after the data conversion is done. Associated operating programs are of the Experimental Physics and Industrial Control System (EPICS) platform. The resulting digital data is converted to beam charge and current information and displayed on the workstation screen. The programs provide mouse-controlled operation for system setup and control.

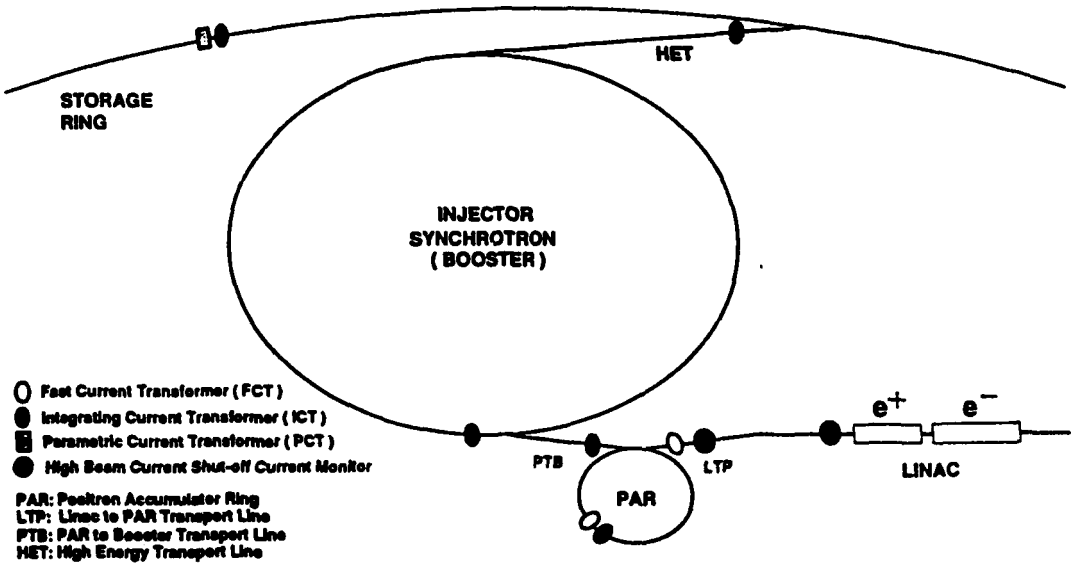


Fig. 1 Locations of beam current monitors in the APS

Beam Current Sensors

The beam current sensors installed, except those in the linac, consist of two types of current transformers: fast current transformer (FCT) and integrating current transformer (ICT), both manufactured by Bergoz. The FCT is a passive AC transformer with a 1-ns rise time. The FCT is installed in the Positron Accumulator Ring (PAR) for observing the bunch length down to several nanoseconds and in the linac to PAR transport line (LTP) for measuring the beam charge and peak current. The FCTs output can be expressed as:

$$U_{out}(t)=\frac{R_o}{N}i_b(t); \quad \textit{then the beam current } i_b(t)=\frac{N}{R_o}U_{out}(t) \quad ,$$

where $U_{out}(t)$ is FCT output voltage, $i_b(t)$ is beam current, R_o is FCT output termination resistance, and N is the number of turns.

The ICT is a passive AC transformer designed to measure the total charge in a very short beam pulse with high accuracy. Its output can be expressed as:

$$\int U_{out}(t)\,dt = \frac{R_o}{N}\int i_b(t)\,dt; \quad \textit{then the total charge} \quad Q = \int i_b(t)\,dt = \frac{N}{R_o}\int U_{out}(t)\,dt \quad ,$$

where $U_{out}(t)$ is ICT output voltage, $i_b(t)$ is beam current, R_o is ICT output termination resistance, N is the number of turns, and Q is the total charge.

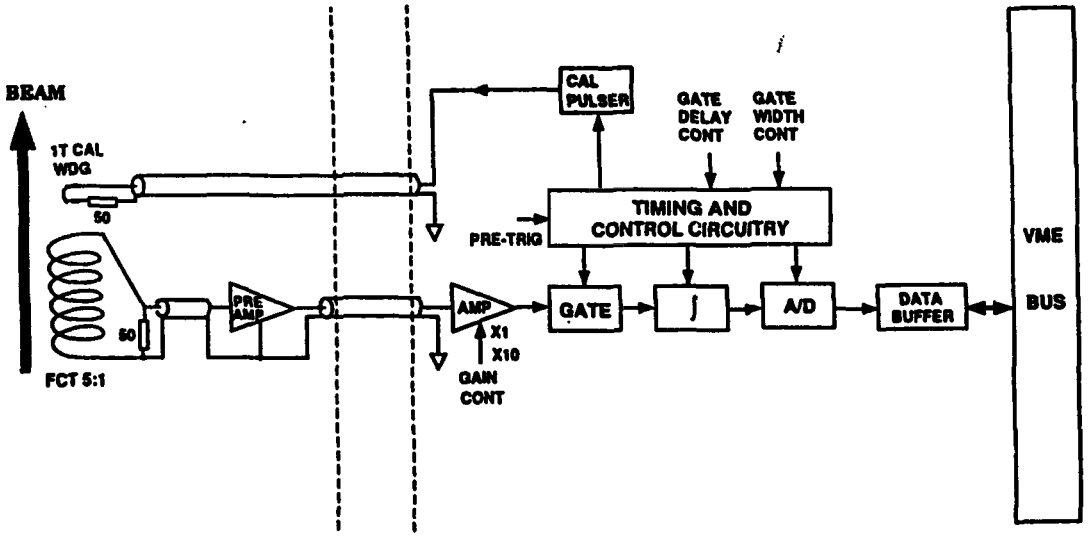


Fig. 2 Block diagram of the VME current monitoring electronics module

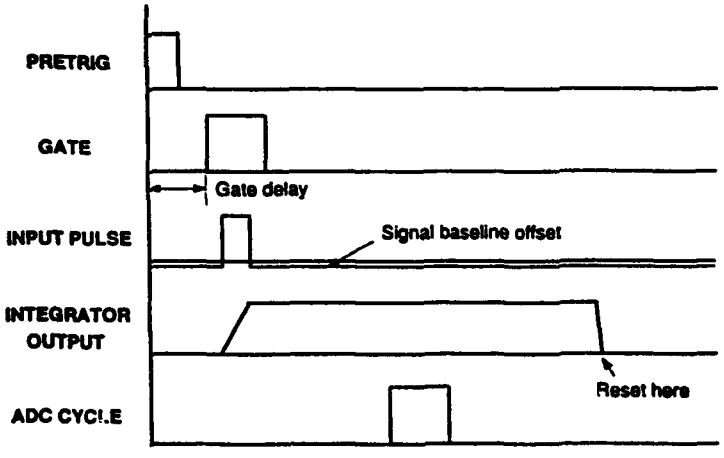


Fig. 3 Timing diagram

The Measurements of Total Charge, Peak Current, and Average Current

An ultrafast, high precision gated integrator has been developed to accurately calculate the transformer's output waveform area that is proportional to the total beam charge, and to hold its output DC level for digitizing. This gated integrator provides fast response and high precision by introducing new design approaches. The various circuit errors usually associated with a high speed gated integrator are virtually eliminated. Consequently, the transfer function of an ideal integrator can be used in the measurements. If the input signal falls within the gate window of t_2-t_1, then

$$V_o = \frac{1}{RC}\int_{t_1}^{t_2} V_i(t)\,dt \ ,$$

where V_o is the gated integrator's output DC level, $V_i(t)$ is input signal voltage, and RC is the integrator time constant.

The total charge of a beam pulse can be calculated directly from the gated integrator output voltage V_o . Let the ICT's output be connected to the gated integrator's input, then

$$V_o = \frac{1}{RC}\int_{t_1}^{t_2} V_i(t)\,dt = \frac{1}{RC}\int_{t_1}^{t_2} U_{out}(t)\,dt = \frac{1}{RC}\left[\frac{R_o}{N}\int_{t_1}^{t_2} i_b(t)\,dt\right] = \frac{R_o}{RCN}Q$$

$$\text{then} \quad Q = \frac{RCN}{R_o}V_o = kV_o \ , \qquad k = \frac{RCN}{R_o} \ ,$$

where k is the conversion constant.

The gated integrator output DC level V_o is first digitized, and then multiplied by the conversion constant to obtain the total charge data for the display.

To make the system integration easier, the peak current measurement in the LTP is also made by the gated integrator instead of another type of electronics, such as peak detector. The peak current readout is obtained by integrating the FCT output and dividing the total charge data by the linac pulse width. That is,

$$I_b = \frac{Q}{t_w} \ ,$$

where t_w is the pulse width of the linac macropulse.

Since there is only one beam bunch in the PAR or Injector Synchrotron at any time, the average current in the rings can be simply obtained by dividing the total charge of the single bunch by the ring revolution time:

$$\bar{I} = I_b\frac{\sigma}{T} = \frac{Q}{\sigma}\times\frac{\sigma}{T} = \frac{Q}{T} \ ,$$

where I_b is the peak current, σ is the bunch length, and T is the ring revolution time.

Software and Control Interface

The APS control system is based on EPICS, a distributed database-driven control system in use at several accelerator facilities. The charge and current monitor is interfaced to EPICS at the device layer. The device layer provides a standard environment between the driver layer, which accesses hardware, and the database record layer. EPICS provides an extensive set of record types from which a control database may be constructed. The device layer for the current monitor supports three record types: 1) an Analog In record to read the ADC values, 2) a Pulse Delay record to control the monitor's internal gate delay and width timing, and 3) Long In record to provide readback of the delay and gate values. In addition to these three record types, the current monitor database uses Calculation records to convert ADC input values to charge and current, Buffer records to accumulate successive measurements, and Sequence records to control the Buffer records.

The APS timing system provides triggers to the monitor electronics to time the gate-to-bunch arrival. Since the current monitoring electronics does not provide an interrupt to signal a data conversion, the APS event system, part of the timing system, is used in lieu of a monitor interrupt. The event system is capable of triggering processing of specific records. An appropriately timed event is used to trigger processing of the Analog In record that fetches a value from the current monitor. The processing of this Analog In record triggers a cascade of record processing through a link mechanism which converts the input value to charge and current through Calculation records and stores the converted values in Buffer records.

The data collection rate for the LTP and PAR is 60 Hz. Rather than transfer converted values at the collection rate, the samples are accumulated in the Buffer records and transferred to an X-windows based operator interface as a single data set at a 2 Hz rate. This greatly reduces the packet rate on the Ethernet local area network (LAN). The data set is displayed graphically as an xy plot of charge and current vs. bunch number.

In addition to the xy display of charge and current vs. bunch number, the operator interface for the monitors displays the ADC voltage, charge, and current numerically. Slider controls are provided for the monitors' internal gate delay and gate width timing.

Mechanical Design

Figure 4 illustrates the mechanical design for the synchrotron current transformer housing. The transformer is external to vacuum and encased in a copper and Mu-metal multi-layer shell to shield the transformer from external noise. The vacuum chamber is formed by a commercial ceramic break and a welded bellows which provides the protection for the ceramic break. A stainless steel tube with the same

aperture as the synchrotron vacuum chamber is suspended inside the ceramic break and a bellows and is attached to the downstream end flange. A gap of 2mm is kept between the tube and the upstream end flange to limit the bandwidth of the cavity formed by the housing to prevent it from ringing with the beam frequency components. The transformer is supported by three G10 sectors attached to the inner wall of the housing, and is held axially by a G10 ring.

OPERATION AND PERFORMANCE

The charge and current monitors described have been installed and used extensively to support the commissioning and operation of the APS injector subsystems including the PAR, Injector Synchrotron, and beam transfer lines of the APS since February, 1994. The VME gated integrator modules are also installed in the linac to provide beam current measurements and readouts for all Faraday cups and current monitors which use the wall current monitor instead of the current transformer as beam current sensors.

Each system was calibrated prior to operation by injecting the test pulses to a single-turn calibration winding of the transformer to simulate the beam pulses of fixed charges. The timing variables for the gated integrator must also be set properly. The gate delay and width are adjusted so that the beam pulse falls well within the gate window. This control requires adjusting only when the system is installed since the trigger to the beam pulse delay is a constant for a given location. However, if the IOC where the VME electronics card is seated needs rebooting, then both gate delay and width have to be readjusted to the original settings after the rebooting.

Figure 5 shows the typical oscilloscope traces of the LTP current monitor. The electron beam pulse picked by an FCT (middle trace) inside the gate window (top trace) is integrated by the gated integrator to produce an output DC level (bottom trace) proportional to the beam current for the digitizing. The output is returned to zero by a reset pulse after the analog-to-digital conversion is completed so that the gated integrator is ready for next cycle beam pulse.

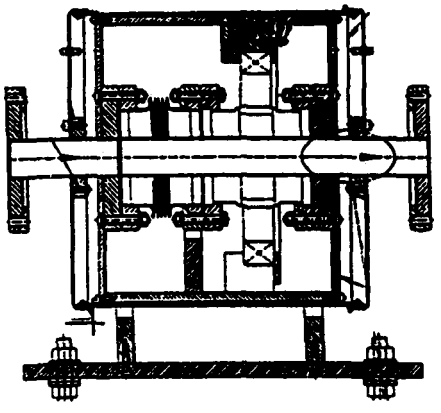
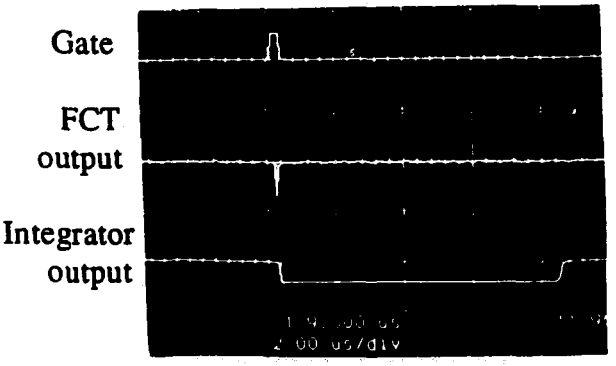


Fig. 4 Mechanical design



Middle trace: 80mV/div
Bottom trace: 400mV/div

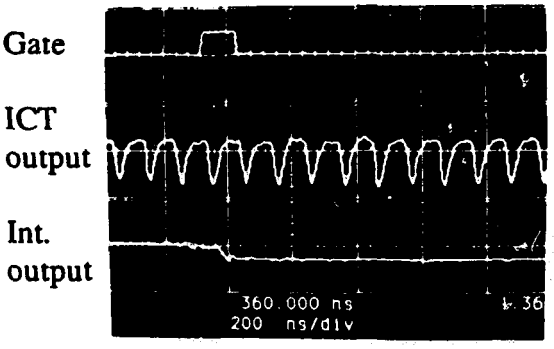
Fig. 5 LTP current monitor signals

The PAR current monitor data is shown in Fig. 6. The small physical size of the PAR determines its high beam revolution frequency. The beam pulse separation seen by the ICT is only 102 ns . Because of this, the ICT output signal (middle trace) shows a large signal baseline offset relative to the signal amplitude. The offset level changes as beam intensity changes. The high performance of the fast gated integrator is well demonstrated here in the single bunch charge measurement. As shown in Fig. 5, the signal baseline is subtracted and only one beam bunch signal is integrated within the 100ns gate window.

Figure 7 shows that the PAR current monitor data is displayed on the workstation both numerically and graphically as an xy plot of charge and average current vs. bunch number. Three linac bunches were injected into the PAR, and the current monitor tracked the stacking of the bunches in the PAR.

To optimize the system resolution with low beam current signal, a programmable AGC amplifier is being added to automatically scale the beam signal so that the gated integrator's output DC level is always close to the full range of the A/D converter.

The system grounding method discussed in (3) was applied to all current monitors installed in the machine and has been proven very effective in reducing the noise.



200mV/div except top trace

Fig. 6 PAR current monitor signals

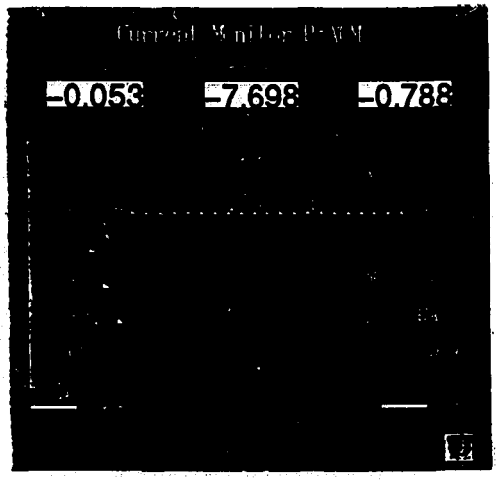


Fig. 7 PAR Current monitor display

REFERENCES

1. K. Unser, "Design and Preliminary Tests of a Beam Intensity Monitor for LEP," Proceedings of the 1989 IEEE Particle Accelerator Conference, Volume 1, p. 71.
2. X. Wang, " Ultrafast, High Precision Gated Integrator," these proceedings.
3. X. Wang, "Design and Initial Tests of Beam Current Monitoring Systems for the APS Transport Lines," AIP Conference Proceedings No. 281, p. 234-241, 1992.