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A FLEXIBLE ANALOG MEMORY ADDRESS LIST MANAGER/CONTROLLER FOR PHENIX*

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A programmable analog memory address list manager/controller has been developed for use with all analog memory-based detector subsystems of PHENIX. The unit provides simultaneous read/write control, cell write-over protection for both a Level-1 trigger decision delay and digitization latency, and re-ordering of AMU addresses following conversion, at a beam crossing rate of 112 ns. Addresses are handled such that up to 5 Level-1 events can be maintained in the AMU without write-over. Data tagging is implemented for handling overlapping and shared beam event data packets. Full usage in all PHENIX analog memory-based detector sub-systems is accomplished by the use of detector-specific programmable parameters -- the number of data samples per Level-1 trigger valid and the sample spacing. Architectural candidates for the system are discussed with emphasis on implementation implications. Details of the design are presented including design simulations, timing information, and test results from a full implementation using programmable logic devices.

ABSTRACT

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Analog memory units (AMUs) play an important role in many physics experiments as data storage elements [1,2,3]. Use of these elements allows proper handling of delays associated with making trigger decisions and digitization latency [3,4,5]. Published methods used for controlling AMU writing and reading have included both direct addressing [3] and serially shifted bit enabling schemes [1,2]. However, special requirements associated with multiple event handling (up to 5) with variable sample number and spacing requires a new architecture.

This paper presents an memory controller designed to provide a solution for all AMU-based detector subsystems of PHENIX -- namely Multiplicity Vertex Detector (MVD), EM Calorimetry (Lead Glass and Lead Scintillator), Muon Identifier (MUID), and Pad Chambers (PC). All subsystems will use a voltage write-voltage read 64-cell AMU per detector channel fabricated in 1.2μm CMOS [6]. Up to 256 detector channels will be controlled by a single AMU address list manager/controller. The controller has several programmable parameters that ensure full applicability to these 5 detector sub-systems: number of samples per valid trigger, and sample spacing specified as the number of beam clocks between adjacent samples. Additionally, the Level-1 trigger delay is programmable. Besides programmability, other special functions are implemented including cell protect mode, address re-ordering, and data tagging. Each AMU must be able to store up to 5 Level-1 qualified events and protect these events while continuously writing to unprotected AMU cells until the events are digitized. After digitization, the address are placed into the available address list in appropriate order. Address reordering acts to reduce the injected noise into the AMU during cell read/write operations. When considering multiple samples and possible multiple Level-1 events, event data packets can become highly interspersed and will require separation. Data tagging allows more straightforward separation and reconstruction of the individual beam events at a higher level in the PHENIX data acquisition system from overlapping and/or shared data. The AMU controller presented in this paper performs these functions at the PHENIX beam clock rate of 8.9 Mhz.

Fig. 1 shows a high-level block diagram for the address list manager portion of the unit. The method employed involves the shuffling of 6-bit AMU addresses. Though this requires larger memory space, it provides some distinct advantages when the special functions associated with multiple event buffering, address re-ordering and data tagging are considered. The basic address list manager is a recirculating loop composed of three memory units. The Level-1 Delay FIFO is used to implement the level-1 trigger delay and can be programmed to be as large as 40μs. After the delay period has passed, the address is placed into the ADC Conversion FIFO awaiting digitization if qualified, or passed to the Available Address FIFO to be re-used. The addresses in both the Level-1 Delay FIFO and the ADC Conversion FIFO are protected from being overwritten. As digitization is completed, the associated address is released, and placed in proper order in the Available Address FIFO for re-use. Another circuit module handles the function of properly tagging the data. By observing the Level-1 trigger signal with knowledge of the programmable sample parameters, the data are tagged as to which event they are associated with (only for the cases where multiple triggers occur and data is overlapping or shared). An additional tag is used to indicate if the data is shared, that is, used in two or more data packets. The sharing function is particularly important since a single AMU cell value cannot be digitized twice with adequate accuracy, and double conversions slow digitization throughput.

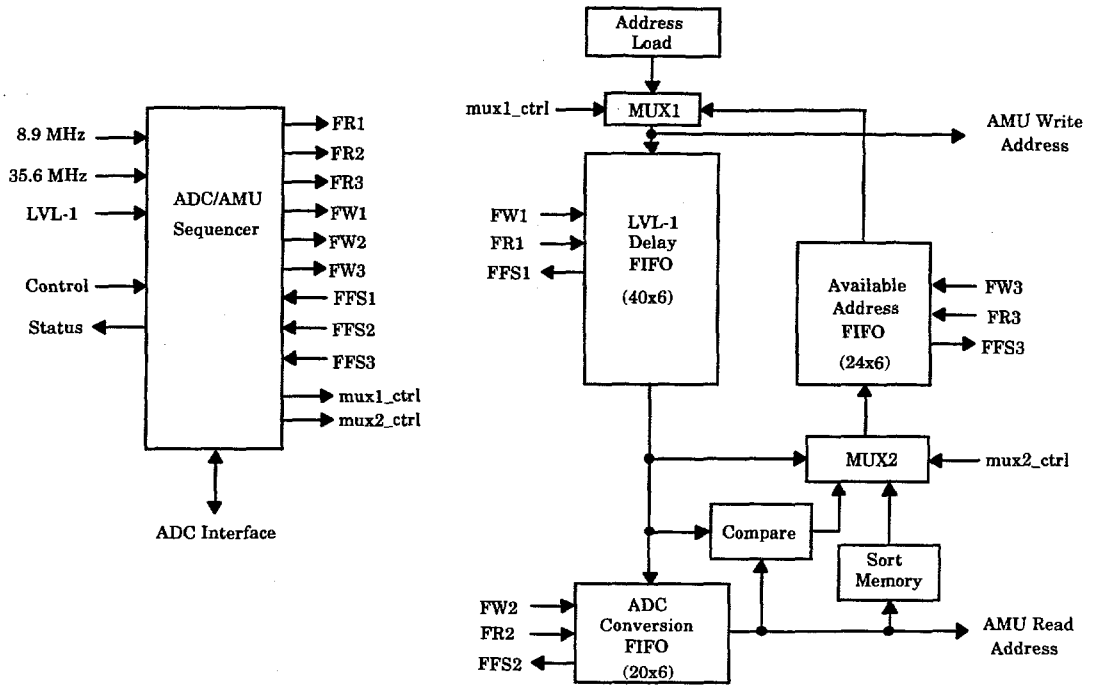

Fig. 1. Address List Manager Block Diagram

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