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Development of a fast pixel array detector for use in microsecond time-resolved x-ray diffraction

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ABSTRACT

A large-area pixel x-ray detector is being developed to collect eight successive frames of wide dynamic range two-dimensional images at 200kHz rates. Such a detector, in conjunction with a synchrotron radiation x-ray source, will enable time-resolved x-ray studies of proteins and other materials on time scales which have previously been inaccessible. The detector will consist of an array of fully-depleted 150 micron square diodes connected to a CMOS integrated electronics layer with solder bump-bonding. During each framing period, the current resulting from the x-rays stopped in the diodes is integrated in the electronics layer, and then stored in one of eight storage capacitors underneath the pixel. After the last frame, the capacitors are read out at standard data transmission rates. The detector has been designed for a well-depth of at least 10,000 x-rays (at 20keV), and a noise level of one x-ray. Ultimately, we intend to construct a detector with over one million pixels (1024 by 1024).

We present the results of our development effort and various features of the design. The electronics design is discussed, with special attention to the performance requirements. The choice and design of the detective diodes, as they relate to x-ray stopping power and charge collection, are presented. An analysis of various methods of bump bonding is also presented. Finally, we discuss the possible need for a radiation-blocking layer, to be placed between the electronics and the detective layer, and various methods we have pursued in the construction of such a layer.

Keywords: Pixel Array Detector, x-ray imaging cameras, time-resolved x-ray diffraction

1. Introduction

The development of high intensity synchrotron x-ray sources has made it possible to perform x-ray diffraction and crystallography experiments on time scales sufficiently short (microseconds) that fundamental biological, chemical, and physical processes may be probed. With the proper detectors and techniques, time-resolved studies should be able to study complicated interactions, such as those involving proteins acting upon substrates.[1,2]

Currently, detectors capable of quantitatively imaging successive, wide dynamic range 2-dimensional diffraction patterns on this timescale do not exist. The current methods of making time-resolved measurements either physically move a detector (i.e. film or image plates) through the diffraction region or rely on electronic techniques. Physical motion techniques are limited in speed and usually produce streak images which can be difficult to analyze. The frame rate of CCD detectors is limited by the slow decay of x-ray sensitive phosphors and the limited readout rates of the CCD electronics. A bright spot on a fast x-ray phosphor, such as Gd_2O_2S:Tb requires several milliseconds to decay in intensity by a factor of 10^{-4}.[3] High speed CCD cameras, such as those built at David Sarnoff Research Laboratories (Princeton, NJ) are capable of a 12-bit dynamic range at a framing rate of almost 1kHz.[4] The limited speed results from the need to serially digitize the stored intensity at each pixel, and can only be improved by dramatically increasing the parallelism of the design.

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By using the technique of Pixel Array Detectors (PADs),[5] pioneered for use with infrared sensors and high-energy physics tracking detectors, we have developed a preliminary design for an x-ray detector capable of storing 8 sequential frames with a time-resolution of five microseconds. The design goals are: a) five microsecond framing; b) 10,000 x-rays/pixel well-depth; c) noise less than one x-ray; d) low storage droop-rates, which allow long integration times and moderate readout rates; and e) negligible frame-to-frame and pixel-to-pixel crosstalk. The PAD is a two-layer device, consisting of an x-ray sensitive array of photodiodes (each 150 by 150 microns square) bonded to a pixelated CMOS electronics layer (with pixels limited in size to the same area as the detector pixels). Each pixel of the electronics layer integrates the current generated by the x-rays converted in the photodiode, and stores the result as a voltage in one of eight capacitors, to be read-out after the last frame is stored. By waiting until the end of the experiment, the framing speed of the device is limited only by the capabilities of the integrating amplifier.

This format for the detector has several advantages over other fast x-ray detectors which have been proposed using similar technology.[5,6] The detector pixel size is small; the 150 micron pixels are comparable in size to the available synchrotron beams. This results in a small, 15 cm detector, which can be placed close to the diffraction sample. Secondly, the design is a straight-forward application of readily available CMOS technology. The desired performance is achievable without requiring large numbers of layers of electronics or high speed analog-to-digital conversion. Thirdly, the design is for an integrating pixel and, therefore, is not dependent upon the ability to count individual x-rays. Since a one percent measurement of the intensity in any pixel requires 10,000 x-rays, this would severely limit the ultimate speed of the detector. Finally, the simplicity of the design will allow the entire device to be built at the cost of only a few wafer fabrication runs.

2. Status

Currently, the development consists of two parallel design efforts. First, we have fabricated and tested three successive generations of designs for the electronics layer. The test chips consist of arrays of the electronics pixels, each of which is AC coupled to a pin of the chip. A negative step function of the voltage on the input pin will inject electrons into the electronics for the associated pixel, mimicking the output of a p-type photodiode. This paper focuses on the results from the latest design, which was made using the Hewlett-Packard 1.2 micron CMOS process offered by the MOSIS service of the Information Sciences Institute at the University of Southern California. The second part of the project involves the design of the x-ray sensitive photo-diode. We have modeled the diode layer, and are in the process of manufacturing test photo-diode arrays at Princeton.

These arrays will be tested and bonded to a fourth test chip which we are currently fab-

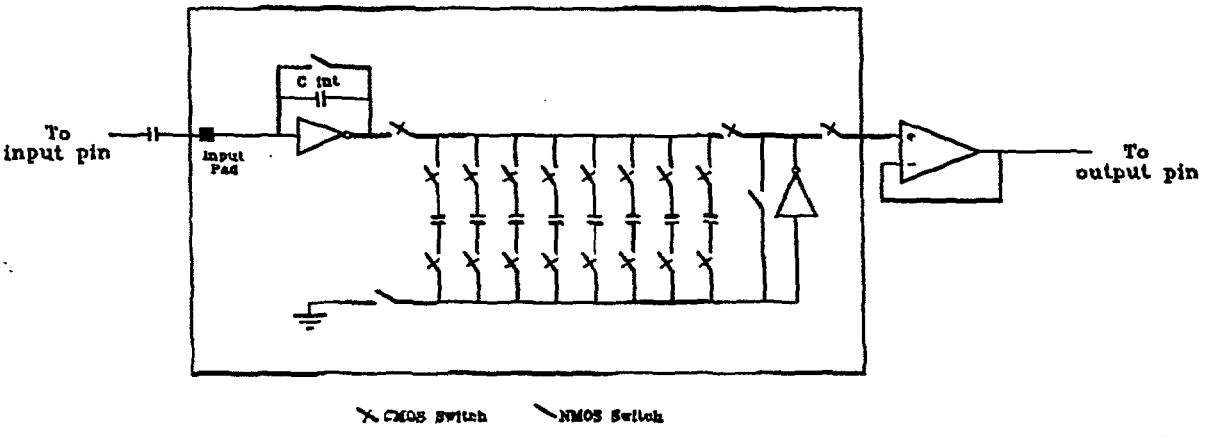

Figure 1: The schematic for a single pixel of the electronics layer. The AC coupling capacitor and the output buffering op-amp are not part of each pixel, but are instead added to provide an interface between the electronics to be tested and the pins of the chip.

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ricating using the same HP 1.2 micron process. Instead of AC coupling the pixel inputs to the pins of the chip, each pixel will be connected through the overglass coating of the chip to a pad which will provide a location for bump-bonding to the diode layer. The fourth chip will also contain the necessary modifications needed to accommodate the n-type photo-diode layer, which sources holes instead of electrons.

3. Electronics Layer

The schematic for the electronics layer of the third chip is shown in Figure 1. This chip was designed for integration of electrons, and the conversion to integration of holes which was incorporated in the design of the fourth chip is straight-forward. Since the tests which we are reporting were performed on the third chip, the discussion will be based on the integration of electrons. In addition, all tests were performed by inserting a negative voltage step onto the pin-side of the AC coupling capacitor which is placed between the pin and the input to the circuit.

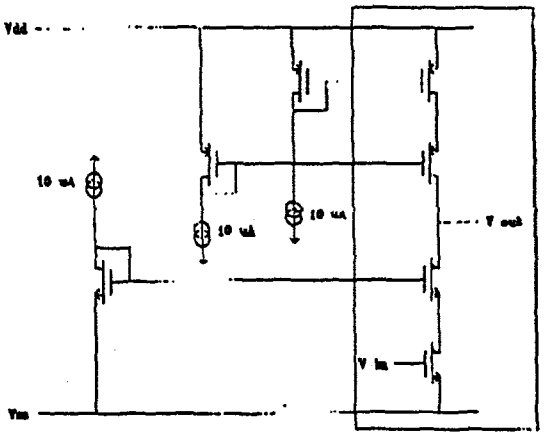

Figure 2: Schematic for the cascode amplifiers. Only the transistors within the box are placed within the pixel electronics.

The charge which appears at the input node is integrated on the integration capacitor by the inverting amplifier. The inverting amplifier is a simple four MOSFET cascode inverting amplifier (see Figure 2). The voltage transfer function is shown in Figure 3. This was measured for a test amplifier which had its input directly connected to a pin of the chip. The open loop gain of the amplifier, near the closed-loop quiescent point, is 1900, resulting in a full-scale voltage swing for an input voltage change of less than 3mV. The amplifier is capable of an output current between 5 and 10μA. Provided that the input current is not higher than this, the input node voltage will be held between 0.925 and 0.928 V by the feedback. Neglecting this spread in voltages (which is roughly linear with stored charge), the output voltage will simply be $Q/C + V_0$, where C is the capacitance of the integration capacitor, 2.02pF, and V_0 is the input node voltage. The operating range of the amplifier is from this quiescent voltage to about 4.3V. This gives a well-depth of approximately 3.3V, which gives a charge measurement capability of 41.5 million electrons. This corresponds to roughly 12,500 12keV x-rays (3287 e⁻/12keV x-ray). When the amplifier begins to saturate, the voltage of the input node will start to fall. This is not a dangerous situation, however, since the junction between the substrate and the reset switch is essentially a diode, and the voltage will never be able to fall below one diode drop below ground. The data will also not be affected, since the output voltage of the amplifier will simply stay at the amplifier's top rail.

When driving a 5pF load, the amplifiers are capable of a slew rate of 0.6V/μs. The full load on the input amplifier is conservatively estimated to be 3pF, it should be able to slew while maintaining the quiescent voltage of the input node at a rate of 1V/μs. This corresponds to an x-ray input rate (again at 12keV) of 3800 x-rays/μs, and a minimum full-well integration time of 3.3μs. The integration capacitor is cleared by closing the input reset switch. This

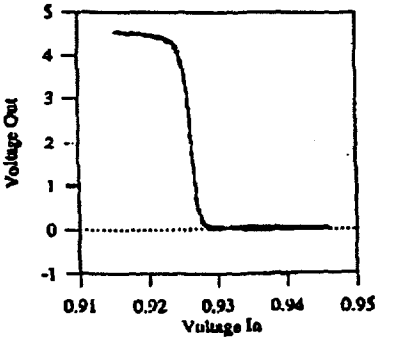

Figure 3: Voltage transfer function for the cascode inverting amplifiers. The open loop gain is 1900 near the quiescent voltage.

discharges the capacitor very rapidly, and, within 300ns, the amplifier settles to its quiescent output voltage.

With the input reset and write enable switches closed, the CMOS switches around the first storage capacitor are closed. The input reset switch is then opened, and the signal from the diode is integrated for the desired period of time. At the end of the integration period, the storage capacitor CMOS switches are opened, leaving the capacitor with the integrated voltage. The input reset switch is then closed, and the process is repeated for the other seven frames. During integration, the voltage for the other plate of the storage capacitor can be set by one of two methods. One option is to close the grounding switch; this will store the full $Q/C + V_0$ on the capacitor. The other option is to set the bottom voltage by closing the output reset switch. This uses the feedback quiescent voltage of the output amplifier, which is identical to the input amplifier, to store only Q/C on the capacitor.

During readout, the opposite procedure is used. With the write enable switch open and the read enable switch closed, the output amplifier is reset by closing its reset switch. The switch is then opened. The small charge injection which results causes the amplifier to slew to its top rail. The storage capacitor switch of the first capacitor is then closed, and the amplifier slews to a final voltage of V_0+V_1 where V_1 is the charge stored on the storage capacitor and V_0 is the quiescent voltage of the output amplifier. Thus, by setting the voltage on the capacitor using the output amplifier feedback method, it is possible to make use of the full voltage range of the amplifiers. In the next generation chip, the grounding switch is connected to an adjustable voltage instead of ground. This will allow the bottom voltage to be set at V_0 without having to rely on the low current capacity of the output amplifier. The technique of slewing the amplifier to the top rail avoids a problem which would otherwise occur when connecting a capacitor with a large stored voltage. If the voltage on the capacitor is greater than V_0, the relatively slow slew rate of the output amplifier (it is driving a load of approximately 5pF) would result in the bottom plate being pushed to a voltage below ground. At higher voltages this would cause the substrate to become forward biased with respect to the sources and drains of the n-MOSFET in the CMOS switch. This would clearly ruin the accuracy of the charge measurement. The slewing technique guarantees that this situation will never occur by keeping the top plate always at or above the voltage which was used to set it.

The capacitors in the HP 1.2μ process are made by implanting a region of the substrate before the oxide is grown to make the one capacitor plate, growing the oxide, and then putting down a layer of polycrystalline silicon to form the other plate. The charge on the bottom plate of each capacitor is therefore somewhat sensitive to fluctuations in the voltage of the silicon substrate. However, when the storage capacitor switches are open, the charge on the polysilicon plate is fixed. The charge measurement system used during both the input and output cycles effectively measures the charge on the input node

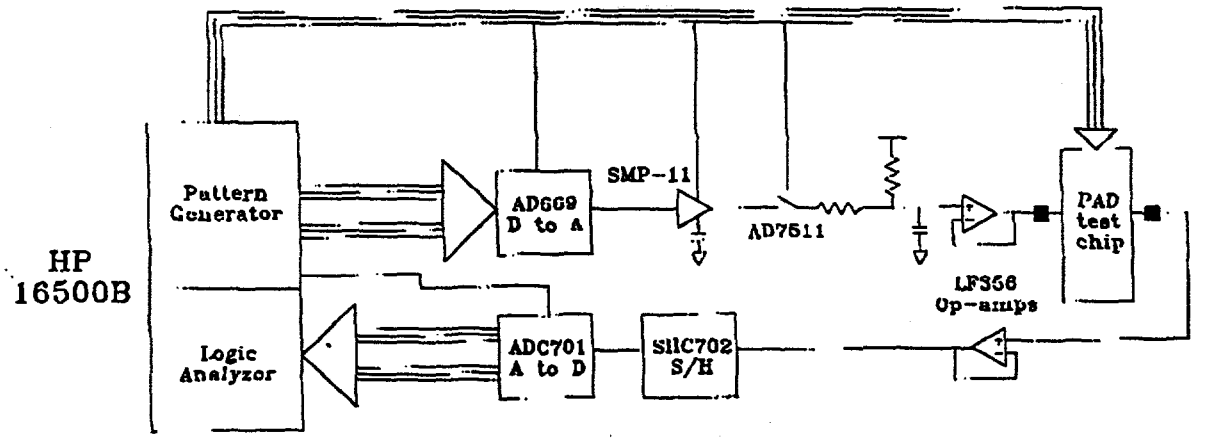

Figure 4: Block diagram for the pixel electronics test. The pattern generator module of the HP 16500B is used both to program the D/A converter and to control the switching of the PAD test chip. The logic analyzer module is used to collect the data from the A/D converter.

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of the amplifier, which places the appropriate opposite charge on the other plate of the capacitor in question. This led us to design the circuit so that the polysilicon plate of the integration capacitor is connected to the input of the input amplifier, and the polysilicon plates of the storage capacitors are connected to the input of the output amplifier (through the appropriate CMOS switch). Note that the plate referred to as the 'bottom' plate of the storage capacitor is actually the physically higher polysilicon plate.

The circuit was tested using a Hewlett-Packard 16500B pattern generator/logic analyzer, combined with an Analog Devices AD669 16-bit digital-to-analog conversion chip and a Burr-Brown ADC701 16-bit analog-to-digital conversion chip. The functional schematic is shown in Figure 4. The DAC is set to a specific voltage between 0 and 5V by the pattern generator. This signal is sampled by one of three Analog Devices SMP-11 sample and hold chips. This allows three signals to be multiplexed into the test chip (in order to test different pixels at the same time). The sample and hold signal is connected through an Analog Devices AD7511 CMOS switch to a resistor to +5V and a simple RC low-pass filter. Thus, by closing the switch, a step function from +5V to the sample and hold voltage is generated at the input to the op-amp. The filter is used to limit the maximum current into the pixel. The op-amp is arranged as a simple follower, buffering this circuitry from the input pin of the chip. Likewise, the output pin of the chip is connected through an op-amp follower to the ADC chip (which, for historical reasons, is arranged to digitize a signal from 0 to 10 V, with 64K corresponding to ground and 0 corresponding to 10V). When the input signal is connected directly to the output buffering op-amp, The performance of the circuit with the input signal connected directly to the output buffering op-amp is as shown in Figure 5a. The external circuitry is linear, with a non-linearity less than its readout noise.

The individual pixels were tested by sequentially placing eight voltage steps on the input pin to the chip, while opening and closing the pixel switches using the function generator. Each frame of the pixel was stepped through its entire range, with several hundred repetitions at each input step value. The output as a function of the input step size for the first frame of a typical pixel is shown in Figure 5b. There was no significant variation from pixel to pixel. Each frame

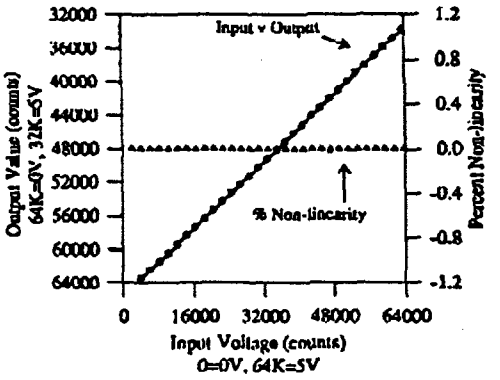

Figure 5a: The performance of the test equipment. The output is extremely linear, with a non-linearity less than its readout noise.

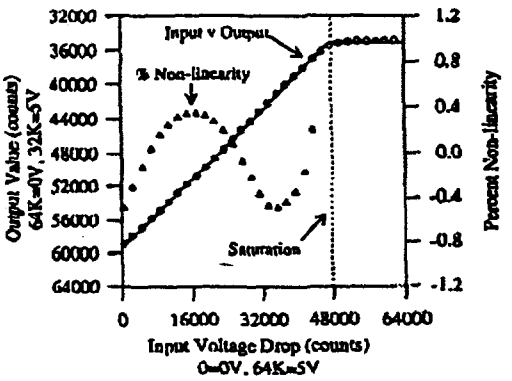

Figure 5b: The performance of the test pixel. Below saturation, the output non-linearity is always less than one percent.

showed roughly the same functional dependence, but there was a small systematic shift (roughly 100 counts). This results from a slight differences in stray capacitance due to an asymmetry in the layout of the switch control lines which will be eliminated in future designs. The dependence is quite linear, with a plateau at high input voltage steps. The data was fit to a sloped line followed by a horizontal plateau. The resulting non-linearity is also displayed on the graph. Aside from the saturation region, the linearity is reasonably good, with a non-linearity always less than one percent of the full scale. More importantly, the fluctuation is stable with time and it should be possible to perform calibrations to eliminate both the non-linearity and the pedestal

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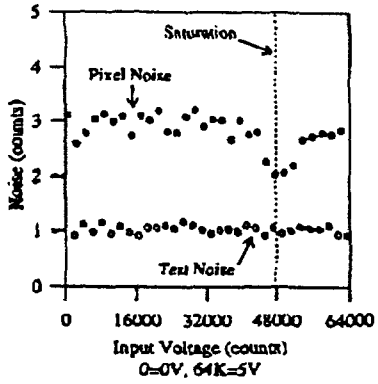

Figure 6: Noise performance. The noise in the test electronics is only at the one count level. The noise in the pixel electronics is three counts, and is flat except immediately around the saturation level.

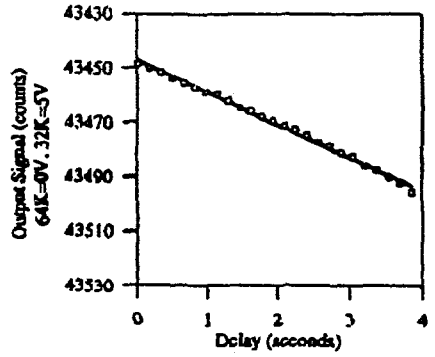

Figure 7: The capacitor droop. The storage capacitors showed a droop rate corresponding to an RC time constant of 1400 seconds.

for each frame of each pixel. The distribution of the digitized output values for each input value was roughly gaussian, so the standard deviation of the points was used as a measure of the noise. The noise performance is graphed in Figure 6.

The pixel electronics noise is three counts and, outside of the region where saturation begins, is independent of the size of the voltage step. Likewise, the read noise of the test system was one count and independent of the signal value. Since the inherent noise of the electronics is added in quadrature to the noise of the test circuitry to produce the three counts, the true electronics read noise is 2.8 counts. This corresponds to a noise of 1.6 12keV x-rays.

The droop associated with each storage capacitor was measured by varying the delay was filled with a fixed value. Then, the between storage and readout. Each of the eight capacitors capacitor to be tested was refilled with a new value. After the delay, this capacitor was also the first capacitor to be read out. The results of the test are shown in Figure 7 for the first capacitor. Each of the other 7 capacitors showed similar results. The droop rate is extremely slow, and the RC decay curve can be approximated as a linear loss of roughly 0.07% per second. This corresponds to an RC time constant of roughly 1400 seconds. This demonstrates that readout times of less than one second should not be problematic. In addition, with proper calibration, exposure times of several seconds should be feasible.

Finally, the crosstalk between capacitors within a pixel was measured. For each measurement, the capacitor to be studied was filled with one value, while the other seven capacitors were filled with another value. The value stored in the other seven was then changed for the next measurement, while refilling the capacitor in question with the same value. By changing the value in the other seven capacitors through the entire range of possible values, the dependence of each capacitor upon the values in the others was measured. The results for a typical capacitor are shown in Figure 8. The effect is less than one x-ray for any capacitor for the full range of possible values for all of the other capacitors.

The performance of the pixel electronics does show a significant dependence upon temperature. The temperature dependence manifests itself as an independent change in the pedestal

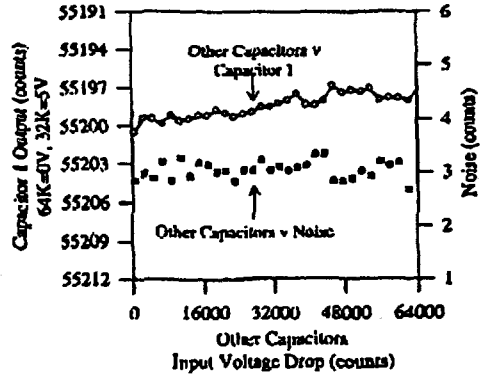

Figure 8: The capacitor-to-capacitor crosstalk.

for each of the storage capacitors. This probably results from a temperature dependence of the charge injection from the CMOS switches. The detector, however, will be operated at a fixed temperature, so this is not expected to be a problem.

4. Diode Layer

The x-ray sensitive photodiode layer will be fabricated on a 300 micron thick wafer of high-resistivity (> 5000 Ω-cm) n-type silicon. The thickness of the layer was chosen to limit the parallax for obliquely-incident x-rays. For example, non-diverging x-rays incident upon the detector at an angle of 45 degrees will pass through the detector at that angle, making a track 300 microns wide (passing through at least two 150 micron pixels) with a charge distribution along the track dependent upon the energy of the x-rays. For a realistic, diverging beam, this problem is even more significant. The 300μm thickness provides an absorption efficiency of 77% for normally incident 12keV x-rays.

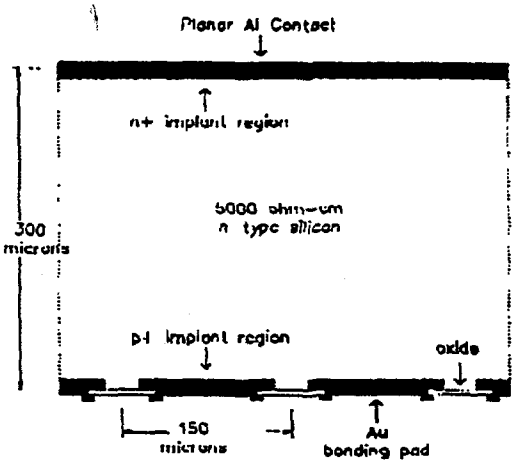

Figure 9: Cross-section of the diode layer. The bonding pads are located on a 150 micron square grid.

The design is a standard configuration for photodiodes in n-type material. The top surface consists of a metal contact (coating the surface) on top of a uniform phosphorus implant. The bottom layer consists of pixels of p-type implants on a 150 micron square grid. Each of these is contacted to a metal pad which will be used for the bump bond to the electronics layer. A back-bias voltage of 70 volts should be sufficient to deplete the full 300μm thickness of the diode. Thus, when an x-ray converts in the depletion region, the electron-hole pairs will be quickly separated with the holes being swept to the bonding pad (and into the electronics). N-type diodes were selected in order to take advantage of two different features of the material. First, the difference in mobility between electrons and holes in the silicon allows full depletion at a much lower voltage than p-type material. This lowers power consumption and reduces the danger of a catastrophic breakdown in the detective layer. Secondly, radiation damage will tend to positively charge the oxide between the pixels on the backside. This results in reduced crosstalk between the pixels, whereas for p-type material it would increase the surface leakage currents.

5. Bump-bonding Issues

The electronics layer will be bonded to the detective layer using standard bump-bonding techniques. Currently, we are considering two different methods. For the fourth chip, with 24 connections, a gold ball method offered by Kulicke-Soffa (Willow Grove, Pennsylvania) will be used. A modified wire bonder places a gold ball upon each of the gold pads of one of the layers. The pieces are then aligned and pressed together. With moderate heat, the gold balls will weld to the two gold pads making electrical contact. For larger projects we expect to use a solder bump process. In this process, a solder bump is lithographically placed upon the bonding pads of each layer. The two pieces are then heated above the melting temperature of the solder, aligned, and pressed together. With careful inspections, it should be possible to achieve a defect rate as low as one in 3000^7, which would translate to 333 bad connections in a one million pixel device.

6. Radiation Damage

The high radiation environment in which the PAD is expected to be used suggests the possibility of a serious degradation in the performance of the CMOS electronics in a relatively short period of time. The electronics layer, unlike the detective layer, is not at all radiation hard, and a dose of 10,000 Rads in this layer could be fatal to the device. In addition, the conversion of an x-ray in the transistors or the storage capacitors of any given pixel could result in a

spurious reading. Fortunately, the x-rays with the highest probability of being absorbed in the oxide of the electronics are also those for which the detective layer is the least transparent. A simple calculation shows that, for a 300μm detective layer, the maximum absorption of x-rays in the electronics will occur at roughly 13.5keV. At this energy, each x-ray incident upon the face of the detector will deposit $3x10^{-6}$ Rads in the oxide of the electronics. Thus, each pixel should be able to withstand about $3x10^{9}$ incident x-rays before failure. In normal operation, provided the detector is not exposed to the direct beam, this should be sufficient for a reasonable detector lifetime. Furthermore, these calculations do not account for the high x-ray absorption of the gold pads and the gold or lead bump. Thus, $3x10^{9}$ x-rays/pixel is a lower limit for the maximum allowable dose. A radiation-hard CMOS process might raise this threshold by several orders of magnitude.

However, low dose damage to the electronics could cause a loss in quality of the oxide. This could manifest itself as a worsening of the capacitor droop rate. In addition, the spurious event rate could be too high for reliable operation. Should these conditions become apparent in prototype detectors a third, radiation blocking layer could be placed between the two layers. Such a layer would need to provide one million feed-throughs on a 150μm spacing. A preliminary design for the blocking layer involves filling the holes in a lead glass capillary plate (manufactured by Collimated Holes, Inc., Campbell, California) with gold and solder, and lithographically depositing gold bonding pads on both sides. Unfortunately, such a layer would have a different coefficient of thermal expansion than the two silicon layers, which could cause difficulties in the solder bonding. A method which might provide an intermediate degree of protection without these problems would be to make the gold bonding pads on both the electronics layer and the detective layer several microns thick. These pads cover a large fraction of the area of the electronics pixels and could be used as radiation shielding.

7. Conclusions

The performance of this latest test chip suggests that this design, modified to collect holes instead of electrons, will work as the electronics for the PAD. It provides low-noise, eight frame signal integration, storage and readout. There is no significant cross-talk between frames, and the storage droop is quite low. All nonlinearities and pedestals are stable with time, and should be removable with accurate calibration.

We are now building a detector which consists of a 4 by 4 array of pixels, with an additional four detective pixels attached to test structures in the electronics layer. This will be an x-ray sensitive device, which should allow verification of the test results described above as well as tests of designs for the detector and a measurement of pixel to pixel crosstalk. Once we have a working 4 by 4 prototype, the design will be scaled up to a 100 by 100 pixel device.

Such a device should allow us to investigate the difficulties of large scale integration and will hopefully lead to a design for a full 1,024 by 1,024 pixel detector. In addition to the concerns already discussed, integration on this scale raises other issues. Since such a detector will be 15cm on a side, it will be necessary to tile together several pieces of both layers. This will require structural support which may be provided by the radiation blocking layer if it is needed. Also, the CMOS electronics will have to be designed with small sub-cells (roughly 15mm on a side) to accommodate the limited reticle size in the fabrication process. All of these problems are tractable, and further development efforts should lead to a working PAD for high speed time-resolved x-ray diffraction.

8. Acknowledgments

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