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DESIGN FOR A FET BASED 1 MHz, 10 kV PULSE GENERATOR

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Abstract

A pulse generator consisting of a coaxial cable and a high voltage modulator, incorporating two stacks of Field-Effect Transistor (FET) switches operating in "push-pull" mode, has been designed and built. The modulator generates a continuous, unipolar, pulse train at a fundamental frequency of 1 MHz and a magnitude of 10 kV. The rise and fall times of the pulses are less than 39 ns. The two stacks each utilize 14 FETS, which are individually rated at 1 kV. The design incorporates a low-loss coaxial cable on which pulses are stored. Extensive PSpice simulations have been carried out to evaluate various design options. Subsequent measurements on the prototype pulse generator confirm the PSpice predictions.

I. Introduction

There is an application at TRIUMF for an electric field kicker system which can generate −9 kV pulses at a fixed repetition rate of approximately 0.923 million pulses per second (continuous)[1]. The specifications for the kicker system call for field rise and fall times of not more than 39.4 ns (10% → 90%), and a pulse with a flat-top duration of approximately 178 ns. The design of the modulator has been carried out for 10 kV unipolar pulses, and a repetition rate of 1 million pulses per second (continuous) [referred to as 1MHz in this paper]: unless specified otherwise, the ratings given in this paper are for 10 kV pulses at 1 MHZ.

A novel high-voltage modulator, developed for the now defunct KAON Factory, generated unipolar 7 kV pulses with rise and fall times of approximately 100 ns, at a repetition rate of 1 MHz (continuous)[2]. This modulator utilized two tetrodes, operating in push-pull mode, as the switching elements, and the pulses were stored on low-loss coaxial cable. The rise and fall times were limited by the high stray capacitance associated with the tetrode whose cathode was connected to the coaxial cable[2]. A FET based high-voltage modulator has recently been designed and built which generates 6 kV pulses at a repetition rate up to 20 kHz, and a pulse width continuously variable in the range 250 ns to 1 s[3],[4],[5]. The measured rise and fall times were approximately 30 ns. The design of the 10 kV, 1 MHz, modulator is based on the design of both the tetrode[2] and the FET 6 kV[3],[4],[5] pulse generators. The latest high voltage modulator consists of two stacks of FET switches operating in push-pull mode, which can generate 10 kV pulses at 1 MHz (continuous). This paper details the electrical design of the high-voltage modulator, and presents predictions from PSpice[6] analyses.

II. General Electrical Design

A low-loss coaxial cable with a characteristic impedance of 50 Ω, and a one-way delay of approximately 540 ns, will interconnect the FET based high-voltage modulator and a set of deflector plates. The coaxial cable will physically remove the modulator from the high radiation environment of the TRIUMF cyclotron, where the deflector plates will be situated[1].

The modulator consists of three stages to convert a TTL timing signal to 10 kV pulses. The first stage converts the TTL signal to 130 V; the second stage converts the 130 V signal to ±450 V; and the final stage generates unipolar 10kV pulses. A negative pulse is required for the application at TRIUMF, but the modulator can equally well generate positive polarity pulses. The two stacks of the final stage each consist of 14 modules (Fig. 1). In order to obtain a realistic prediction from the PSpice simulations, all known parasitics are simulated: for clarity parasitics are not shown in Fig. 1.

The 14 modules of the pull-up stack are labelled UP1 through to UP14 in Fig. 1; UP1 is at the ground end of the stack, and UP14 is at the output end. The 14 modules of the pull-down stack are labelled DN1 through to DN14 (Fig. 1); DN1 is at the high-voltage DC end of the stack, and DN14 is at the output end. Fig. 1 shows two sets of 14 resistors whose nominal value is 24 Ω in the pull-up stack and 36 Ω in the pull-down stack: these resistors interconnect the source (OUT-) of one module with the drain (OUT+) of the adjacent module. The values of these resistors are a compromise between excessive rise and fall times of the output pulse, and both excessive drain current and dissipation in the high-voltage FETs. The high-voltage FET utilized in

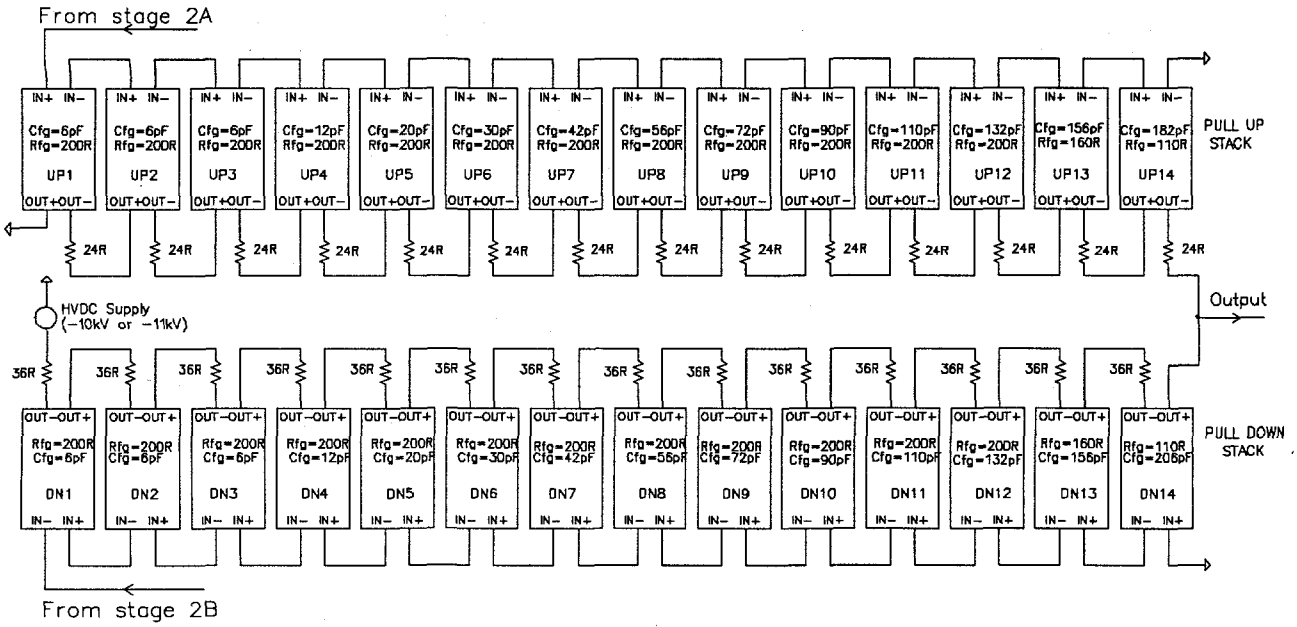

Fig. 1. Schematic diagram of final stage of modulator

each module of the pulse generator is the APT1004RBN[7]. At 25°C the APT1004 FET is rated at 1 kV and can handle a pulsed drain current of 17.6 A[7]. The APT1004RBN has a rated power dissipation capability of 180 W at a case temperature of 25°C: above this case temperature the dissipation capability is reduced[7].

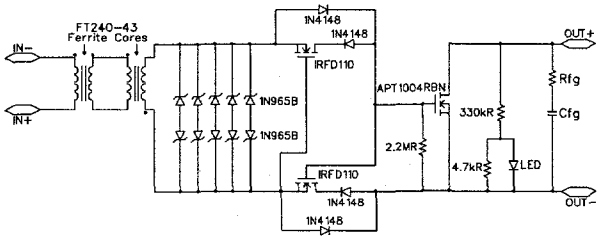

Fig. 2. Schematic diagram of each final stage module

The details of switch modules UP1 through to UP14 and DN1 through to DN14 are shown in Fig. 2: the design is basically the same as the design of the modules employed for the 6 kV, 20kHz FET modulator[3],[4],[5]. However there are some differences, which are described in this paper.

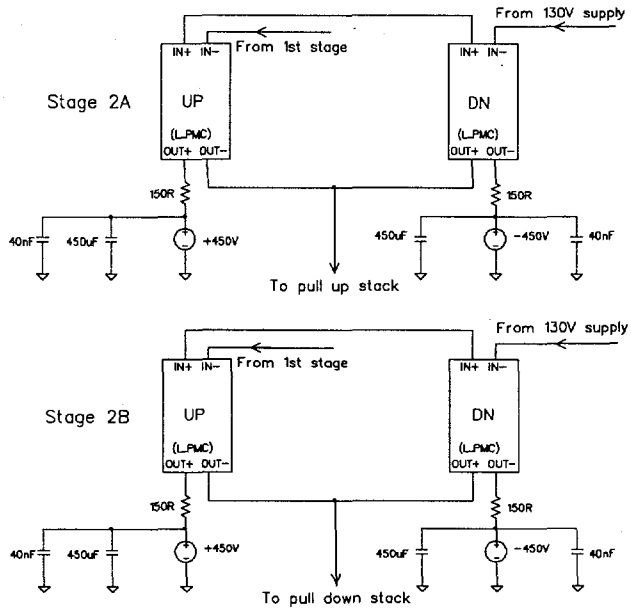

Fig. 3. Schematic diagram of second stage

In order to minimize overlap in conduction of the two stacks of FETs, there is a separate primary winding, and separate second stage driver, associated with each of the two stacks (Fig. 1). The two second stage drivers (labelled 'Stage 2A' and 'Stage 2B' in Fig. 3) are identical to one another, and are driven in parallel by a winding from the output of the first stage. Each second stage has two modules working in push-pull. The second stage modules are basically the same as those of the final stage (Fig. 2), except for the configuration of the ferrite pulse transformer (see section IV).

Although the output of the high voltage modulator will be connected to a coaxial cable, the design calculations are more efficiently carried out without a model of the coaxial cable: when a cable is modelled the stored pulse takes many tens of pulses to build-up towards steady-state (Fig. 5). Hence the CPU time required for the simulation to reach steady-state is significant. Whereas without a coaxial cable the

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simulation reaches steady-state in a few pulses. The HVDC power supply voltage is set to either −10 kV or −11 kV (see Fig. 1): −10 kV is utilized to achieve −10 kV pulses without a storage cable. When a storage cable is installed, as a result of the reflection coefficients between the cable and modulator and losses in the cable, an HVDC supply voltage of −11 kV is required to achieve −10 kV pulses.

III. 6 kV, 20 kHz Modulator

Since the 10 kV, 1 MHz modulator is based on the design of the 6 kV, 20 kHz modulator[3],[4],[5], the PSpice predictions for the 6 kV, 20 kHz modulator were re-examined. The maximum junction temperature rating of the APT1004RBN is 150°C[7]. Calorimetric measurements carried out on APT1004RBN FETs, mounted on various heat-sinks and in a reasonable air-flow, showed that the junction temperature of the APT1004RBN approached 150°C when the power dissipation in the FET was approximately 90 W[8]. However PSpice simulations carried out for the 6 kV modulator, for 1 MHz operation, predicted a power dissipation of 140 W and 50 W for the APT1004RBN FET in module UP7 and UP1, respectively[3]: the mal-distribution of the power dissipation is not a problem at 20 kHz, where the dissipation per APT1004 FET is only a few Watts. Since the predicted voltage grading in the final stage of the 6 kV modulator was fairly close to ideal, and a single primary winding passed sequentially through the ferrite cores of each module (see Fig. 1 of reference[3]), it is not immediately obvious why the predicted dissipation in the APT1004 FET of module UP7 was almost three times greater than for the APT1004 FET in module UP1.

Careful analysis of PSpice predictions for the 6 kV modulator revealed that the high dissipation in module UP7, relative to module UP1, is attributable to the current pulse in the primary of the transformer of module UP7 being significantly reduced in magnitude during the critical period of time when the Miller Capacitance of the APT1004 is being charged. Further investigation showed that the reduction in primary drive was a direct consequence of both parasitic capacitance associated with the pulse transformer and a rapid change in source voltage during switching of the APT1004 FETs. The resulting displacement current was coupled into the primary winding of the pulse transformer and reduced the effective drive on the primary of the transformer of module UP7. The 10 kV, 1 MHz, high-voltage modulator is re-designed (Fig. 1) to take advantage, where possible, of the transients that are coupled through to the primary side of the transformer winding during switching of the APT1004 FETs: this is achieved by modifying the primary winding such that the switching transients increase the primary drive for the modules closest to the output end of the stacks. The net effect of this re-design is to significantly reduce the predicted dissipation in the APT1004 FETs closest to the modulator output, and marginally increase the dissipation in the APT1004 FETs closest to the DC end of the stacks, thus resulting in a reasonably equal dissipation throughout the stacks.

IV. Pulse Transformer

A pulse transformer is utilized at each module to provide electrical isolation between each module and ground[3],[4],[5]. The pulse transformer for the second and final stage modules of the modulator consist of one and two cores, respectively, of FT240-43 ferrite[9].

The APT1004 FET has an appreciable 'Miller' (Gate-Drain) Charge[7]. In order to maintain the switching losses in the APT1004 FET at acceptable levels it is necessary to charge and discharge the Miller Capacitance rapidly. This requires a potential current swing, on the primary side of each of the pulse transformers, of approximately 6 A. The superposition of the 6 A current swing generated by the second stage of the modulator and the displacement current coupled into the primary of the pulse transformer, could cause the gate-source voltage rating of the APT1004 (±30 V) and the IRFD110 FETs (±20 V) to be exceeded. In addition dielectric losses in the ferrite cores closest to the output of the modulator would be excessive. Hence in order to reduce the magnitude of the displacement current associated with the transformer cores, two cores are utilized in the modules of the final stage (Fig. 2). The two cores are electrically in series to the displacement current, thus reducing the effective capacitance to the primary winding. Opera-2D[10] simulations of the ferrite cores show that the capacitance to the primary winding is further reduced if the primary winding passes through the center of the core, rather than being situated adjacent to the outer edge of the core. This prediction is supported by capacitance measurements carried out on the prototype modulator.

A 1 cm wide copper strap is utilized to magnetically couple the two ferrite cores in the modules of the final stage. Another 1 cm wide copper strap is part of a single turn secondary winding. Frequency domain measurements on two closely coupled ferrite cores, with a short-circuit secondary, show that 1 cm wide copper straps result in an acceptable leakage inductance for this particular core configuration. Frequency domain measurements were also carried out on the cores with the secondary winding open-circuit; the PSpice

Optimizer[6] was then utilized to determine the (linearized) core inductance and core-loss resistance which gives the best fit to the measured impedance and phase. Frequency domain measurements have also been carried out on the cores to characterize the dielectric losses: the PSpice Optimizer has been utilized to determine (linearized) values for an equivalent circuit which gives a good fit to the measured data.

V. Voltage Distribution

A. Fast-Grading Components

The parasitic capacitance to ground from each module significantly affects the transient voltage distribution in the final stage. The linearized drain-source capacitance of each of the APT1004 FETs is approximately 90 pF[3], and assuming a parasitic capacitance from drain to ground of 2.2 pF per module[8], the resultant drain-source voltage at the 'pulsed' end of the FET stacks would be more than 4 times larger in magnitude than that at the 'DC' end of the stacks if corrective measures were not taken[5]. In order to equalize the voltage distribution and power dissipation throughout the FET stacks, 'fast-grading' capacitors (Cfg) are connected between the drain and source of each of the high-voltage FETs of the final stage. The following equation is used to determine the required value for each fast-grading capacitor[3],[5]:

$$C_{fg(n)} = C_{m(1)} \sum_{i=1}^{n-1} ik \tag{1}$$

where: $C_{fg(n)}$ is the value of the fast-grading capacitor required for module 'n'; $C_{m(1)}$ is the [linearized] drain-source capacitance of the high-voltage FET; and 'k' is the ratio of parasitic capacitance to ground to the (linearized) drain-source capacitance of the high-voltage FET.

In the equivalent circuit the parasitic capacitance from drain to ground, for each APT1004 FET, was simulated as 1.5 pF. In addition the parasitic capacitance of each ferrite core was 1.5 pF: giving a total parasitic capacitance to ground of approximately 2.25 pF per final stage module (k=0.025), which is very close to the 2.2 pF per module measured[8]. Although $k \simeq 0.025$ results in a virtually ideal prediction for voltage grading, k=0.022 (corresponds to a parasitic capacitance to ground of 2 pF per module) results in a better compromise between the uniformity of the power dissipation and voltage grading. From Eqn. 1, for k=0.022 a fast grading capacitor of 182 pF would be required for modules UP14 and DN14. However the source of DN14 (and the drain of UP14) are assumed to have an additional 2 pF to ground because of their physical location at the ends of the stacks. Hence the required fast grading capacitor associated with module DN14 has a value of 206 pF. Since the additional 2 pF associated with UP14 is on the drain side of the APT1004 FET, i.e on the output side of the modulator, it does not influence the voltage grading, and hence does not effect the value of fast-grading capacitor required. The values of fast-grading capacitors are shown in Fig. 1: all the modules in the final stage of the 10 kV modulator have fast-grading components.

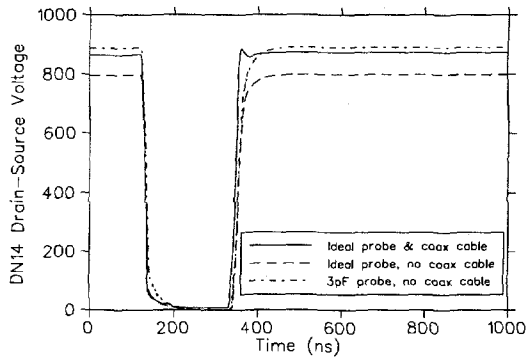

Fig. 4. Effect of probe and coaxial cable upon drain-source voltage of module DN14

In order to avoid excessive drain current, and an excessive contribution to switching losses, in the APT1004 FET during turn-on, it is necessary to connect a 'fast-grading resistor' (Rfg) in series with each fast-grading capacitor[3],[4],[5]. The fast-edges associated with the output pulse of the high-voltage modulator can result in a voltage transient, of approximately 50 ns duration, across the modules nearest to the output of the modulator (Fig. 4). This transient is attributable to a voltage drop across the fast-grading resistors: maximum current flow is associated with the fast-grading circuits at the output end of the stack[5]. In order to reduce the severity of the transient, the fast-grading resistor values are 'graded': modules DN14 and UP14 have a fast-grading resistor of approximately 110 Ω (hot); modules DN13 and UP13 have a fast-grading resistor of 160 Ω (hot); all the other modules in the two FET stacks have a nominal fast-grading resistor of 200Ω (see Fig. 1).

A Tektronix P6015 high-voltage probe, with a 10 foot cable, has an input capacitance of approximately 3 pF[11], which causes a voltage mal-distribution in the final stage during measurements. Hence PSpice simulations have been carried out to assess the mal-distributions caused by using a single P6015 probe

to measure drain and source voltages throughout the final stage, such that the measured voltages can be appropriately interpreted. The extra 3 pF capacitance results in an increase in voltage of approximately 11% across modules 14 (Fig. 4), and a decrease of approximately 3% across modules 1[8]. The measured voltage grading is in excellent agreement with the PSpice simulations which incorporate 3 pF for the P6015 probe[8].

B. Effect of Coaxial Cable

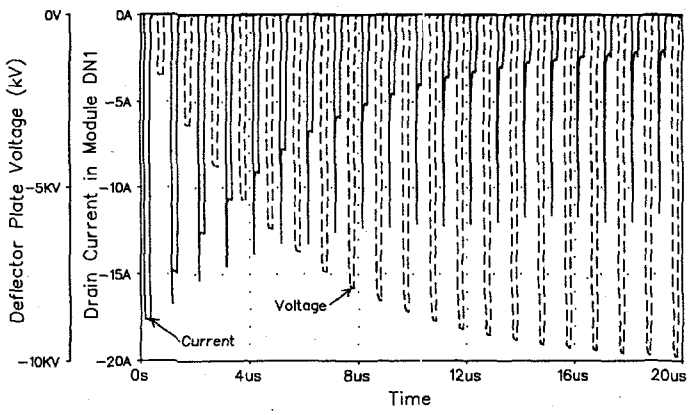

Fig. 5. Voltage build-up and drain current in APT1004 of DN1

As a consequence of the significant source impedance of the modulator, in comparison with the characteristic impedance of the coaxial cable, the pulse stored on the cable requires several tens of cycles to build up to steady-state (Fig. 5). If the HVDC voltage is already at -11 kV (see section II) when the modulator is gated, the pull-down stack will conduct a current of almost 18 A: this current reduces in magnitude as the stored pulse builds-up (Fig. 5).

The back-end of the stored pulses are defined by both the turn-off of the pull-down stack, and turn-on of the pull-up stack. Hence, while the pulse on the cable is building up, the high-voltage FETs in the pull-down stack are required to switch off currents of up to 18 A. As a result of parasitic inductance in the main-current path, forcing the current in the pull-down stack to zero gives rise to an inductive voltage transient across the high-voltage FETs in this stack. Because the turn-off signal propagates from the DC end of the stack, the inductive transient is largest towards the DC end of the stack. The inductive voltage transient decreases in magnitude as the pulse current conducted by the pull-down stack reduces.

The inductive voltage transient is in addition to the voltage transient due to grading of the output voltage pulse throughout the stacks. Initially, when the stored pulse has a relatively small magnitude, the drain-source voltage attributable to the voltage pulse is also small. However as the stored pulse increases in magnitude, the resultant voltage graded through the stack increases. The superposition of the inductive voltage transient and the graded voltage transient is a maximum (~1 kV) for the first pulse following gating of the modulator. In order to minimize the effects of the inductive voltage transient, the modulator is gated before the HVDC supply is turned on, and then the supply is turned-up to -11 kV over a period of seconds: this procedure also limits the dissipation in the APT1004 FETs while the pulse on the cable is building-up.

VI. Predictions

PSpice has been utilized to determine the dissipation in circuit elements such as the APT1004 FETs, resistors, zener diodes and IRFD110 FETs. The rms current flow in the fast-grading components and HVDC power supply has also been calculated.

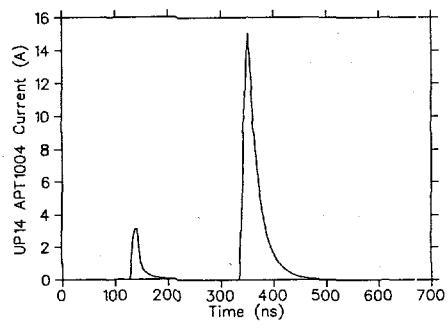

Fig. 6. Current through APT1004 FET in module UP14

Fig. 6 shows the predicted steady-state drain current for module UP14, with the coaxial cable connected: the peak drain current through the APT1004 FET in module UP14 is approximately 15 A. The predicted dissipation in the APT1004 FETs, without a storage cable connected to the modulator, range from 60 W to 78 W in the pull-up stack and 52 W to 65 W in the pull-down stack. With the coaxial cable connected to the modulator output, in order to obtain representative dissipation in the APT1004's, it is necessary to run the simulation for approximately 40 cycles. The predicted 'steady-state' dissipation in the APT1004 FETs range from 50 W to 68 W in the pull-down stack, and from 43 W to 55 W in the pull-up stack. A dissipation of 68 W corresponds to a junction temperature of approximately 120°C[8], which is well within the rating of 150°C[7]. The predictions for dissipation in the pull-down stack, and the fall time of the output pulse (36ns) are in excellent agreement with measurements[8]. However the predicted dissipation in the pull-up stack and rise-time of the output pulse are less than the measured values by approximately

10 W (16%) and 11ns (30%), respectively: this discrepancy requires investigation. With the coaxial cable simulated the predicted rise and fall times are approximately 33% less than without it.

Assuming equal voltage distribution in the FET stacks, and for a given frequency of operation, the power dissipation in any fast-grading resistor in the stack is proportional to the value of the fast-grading capacitor across that module. Under a fault condition, for example one module of the pull-down stack failed to short circuit, worst-case dissipation occurs in the fast-grading resistor associated with module DN14: with the storage cable connected the dissipation is approximately 150 W, and the rms current is approximately 1.2 A.

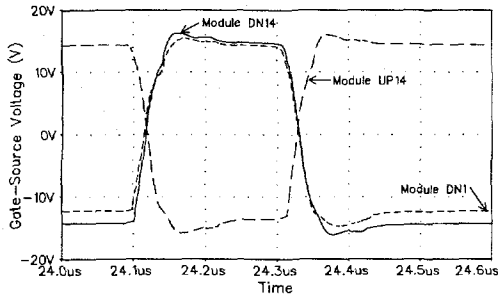

Fig. 7. Gate-source voltage for three modules

Fig. 7 shows the gate-source voltage associated with the APT1004 FETs in modules DN1, DN14 and UP14. Five sets of back-to-back zeners (1N965B) are connected across the secondary winding of each pulse transformer (Fig. 2). Five sets are utilized in order to both reduce the transient impedance, and thus further limit the maximum gate-source voltage of the IRFD110 and APT1004 FETs, and maintain the dissipation in the zener diodes at an acceptable level: only two sets of back-back zeners were required for the 6 kV, 20 kHz version[3]. The predicted dissipation is a maximum for the zeners in module UP14, and is 340 mW per zener. The data-sheet value for the power dissipation capability of the 1N965B zener is 400 mW. The predicted power dissipation in an IRFD110 FET is approximately 0.3 W: the data sheet rating is 1 W.

A second stage voltage of ±450 V (Fig. 3) results in a maximum predicted voltage of approximately 750 V across the APT1004 FETs in the second stage. Increasing the second stage voltage to more than ±450 V has little effect on reducing either predicted rise and fall times of the output voltage pulse or dissipation in the APT1004 FETs of the final stage. The predicted dissipation in the APT1004RBN FETs associated with the second stage is less than 30 W per FET. The 150 Ω resistor banks associated with the second stage power supplies each dissipate up to 1 kW of power: the actual dissipation in a resistor bank is dependent upon the duration of the current pulse in that resistor bank.

The first stage driver has an APT5025BN FET[7], which is rated at 23 A continuous and 500 V: the predicted dissipation in this FET is only a few Watts. However a 25 Ω resistor in the first stage dissipates approximately 150 W. The maximum predicted voltage across the APT5025 FET is approximately 180 V.

The HVDC supply is required to provide approximately 2 A rms of current. The 36 Ω (24 Ω) current limiting resistors in the pull-down (pull-up) FET stack dissipate approximately 160 W (105 W) each.

VII. Conclusion

Extensive PSpice simulations have been carried out for the 10 kV, 1 MHz pulse generator. The circuit design ensures reasonably uniform voltage grading, and power dissipation which is within the rating of the APT1004 FETs. Predicted power dissipation in the pull-down stack and fall time of the output pulse are in good agreement with measurements: there is a discrepancy for the pull-up stack which requires investigation. Predictions of voltage distribution, with and without 3 pF representing a real probe, permit measured voltages to be corrected for the effects of the high-voltage probe. Predicted and measured voltage distributions are in good agreement.

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