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Monolithic Readout Circuits for RHIC

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1.0 Abstract

Several CMOS ASICs have been developed for a proposed RHIC experiment. This paper discusses why ASIC implementation was chosen for certain functions, circuit specifications and the design techniques used to meet them, and results of simulations and early prototypes. By working closely together from an early stage in the planning process, in-house ASIC designers and detector and data acquisition experimenters can achieve optimal use of this important technology.

2.0 Introduction

ASIC use in high energy physics in increasing.[1] Particularly for front end functions where density and/or cost is a constraint, ASICs' ability to trade off functionality, speed, power, and size can result in efficient detector readout. In addition, certain readout functions are very difficult to perform without custom integrated circuitry, e.g. analog pipeline delay. However, monolithic technology also imposes limitations that can restrict achievable performance, and appropriate circuit techniques must be used to get the full advantage from it.

With this in mind, a close collaboration was started between ASIC designers and data acquisition experimenters for the proposed OASIS experiment in December of 1990. We will discuss the system partitioning, and the rationale for setting priorities for ASIC designs in the next section. This will be followed by descriptions of three ASIC designs, including target specifications, key circuit issues, and approaches taken to realize the goals. Finally a brief report of progress and future plans is presented.

1. See, e.g. Proceedings of the First Annual Conference on Electronics for Future Colliders, May 22-23, 1991, LeCroy Corp., Chestnut Ridge, NY

3.0 Experiment Overview

At the outset a description was made, in functional block format, of the readout electronics for each of the seven major detectors of OASIS. The result is sketched in Fig. 1, where the detectors, readout chains, and channel counts are shown. Next, we selected certain blocks as candidates for monolithic integration; those chosen are shown as shaded boxes in Fig. 1. Since about 95% of the channels are in the transition radiation detector/tracker and liquid argon calorimeter, ASICs were considered for all blocks in their readout chains for cost reasons.As mentioned already, the LAr AMU (analog pipeline) cannot be built from commercial components. Among the other systems, the silicon pad multiplicity detector and silicon drift chambers have space constraints, again making ASICs advantageous.

While similarities exist among the front-end blocks of many systems, their requirements (for noise, dynamic range, etc.) differ at the detail level. Hence, there was not enough commonality to try to make any single ASIC fill more than one block. The eleven candidate ASICs could not all be addressed simultaneously with the resources available, so priorities were attached based on system-wide costs; this led to the selection of the three blocks shown with bold outlines in Fig. 1 for custom design. The TRD ADC RAM and L2 PIPE/DATA COMP functions could be implemented with field-programmable gate arrays (FPGA's), while the other LAr circuits could be made with hybrid technology. The three circuits chosen could all be produced in readily available CMOS technology.

4.0 TRD/Tracker

4.1 Detector and signal characteristics

The TRD/Tracker identifies electrons by detecting transition radiation which is emitted as they traverse a foam or foil radiator. In addition, particle momentum is measured for all charged particles through their ionization energy loss dE/dx. Figure 2 shows a schematic cross section of a particle crossing one layer of the TRD/Tracker along with a description of the possible anode current waveforms. For hadrons, only dE/dx charge is produced in the chamber; this drifts to the anodes and produces a current whose duration is proportional to the cosine of the angle of incidence. The current will fluctuate due to the statistical distribution of primary ionization clusters. Electrons with momenta > 0.5 Gev/c can also emit a transition radiation photon in the range of 5 - 25 keV, which has a high probability of being absorbed in the chamber gas. This produces localized ionization that results in a short current pulse of much higher magnitude than the accompanying dE/dx signal.

The characteristics of the TRD/Tracker charge and current waveforms are summarized in Table 1. The readout electronics consists of a charge-sensitive preamplifier, shaper with integration time constant matched to the average diffusive broadening of the drift chamber, and fast ADC. The 4-bit ADC has 12 levels spanning the dE/dx range and 3 levels in the TR region. It takes samples of the waveform every 20 nsec to provide good time resolution of the leading and trailing edges.

4.2 Preamp/shaper

Based on the expected characteristics of the signal waveform as described above, the specifications shown in Table 2 for the preamp/shaper ASIC were developed. The equivalent input noise charge (ENC) is about 1/20 of an LSB on the cathode strips.

Because of the high capacitance of the detector (50 pf for anode wires, 150 pf for cathode strips) and the relatively short shaping time of 70 nsec, this ENC goal is a challenge. In a well-designed preamp/

shaper, most of the noise comes from the preamp input device, so its design and biasing are critical. The following conclusions can be drawn:

- In this shaping time range, channel thermal (white) noise dominates so an NMOS device can be used.
- Minimum gate length should be used.
- An optimum gate width exists based on detector capacitance, but its value may be prohibitively large.
- Once the optimum gate dimensions are chosen, noise is a function of drain current so there is a fundamental noise/power trade-off.
- Careful attention must be paid to gate and substrate parasitic resistances.
- Reverse biasing the source-substrate junction reduces noise by reducing the body-effect transconductance g_{mb}.

It is also important to minimize the noise contributed by the bias sources in the circuit, which can contribute up to 50% of the noise. Additionally, it is important to protect the CMOS input from electrostatic discharge damage in a way that does not add noise.

Figures 3 (a) and (b) show calculated ENC (due to the input NMOS device only) as a function of W_g and I_d, for circuits made in a 2 μm n-well CMOS process. It can be seen in Fig. 3(a) that the noise minimum is a very shallow function of gate width. In Fig. 3(b) one sees that the 2500 r.m.s. e^- goal can be met for the cathode preamp ASIC, but only at the cost of several mA of drain current in the input device; in practice, this circuit will dissipate 15-75 mW per channel. The ENC goal is much easier to meet for the lower-capacitance anode wires.

The circuit of Fig. 4. was designed to meet the requirements for cathode strip readout. It consists of a folded cascode charge-sensitive loop with a long-channel PMOS device biased in the triode region for a high value DC feedback resistor. Device sizes were chosen to minimize noise while maintaining speed and stability. Simulations predict an ENC of 2560 r.m.s. e^- at 70 nsec shaping and 150 pf detector capacitance, with a rise time of 70 nsec and overall power consumption of 22 mW. A similar circuit could serve as an anode wire preamp, but with at least 10 times lower power.

4.3 Shaper

A transfer function with a zero at the origin and 5 equal-value real poles at 9.1 MHz produces a step response that peaks in 70 nsec and has adequate noise rejection. Key design issues for this circuit are:

- Provision of at least two poles per op-amp to minimize power.
- On-chip passive components used to set the time constants have wide manufacturing variations (20% run-to-run) in typical ASIC fabrication.
- The shaper's equivalent input noise voltage should be less than the preamp ENC/C_F (a few hundred microvolts in this case) to minimize its contribution to overall noise.

The circuit shown in Fig. 5[2] was chosen to implement the $1/(1+s\tau)^2$ transfer function. One open-loop pole is contributed by the capacitance at the drain of M3 in parallel with its transconductance and a second is formed by C1 and (R1+R2). In the closed loop, the poles move together to result in a transfer function:

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2. Z. Chang, Low Noise Wide-Band Amplifiers in Bipolar and CMOS Technologies, Kluwer, 1991 pp. 186-188

$$H(s) = \frac{G_0 R1}{(1+G_0 R1) + s(\tau_1+\tau_2) + s^2\tau_1\tau_2} \quad (1)$$

where

$$G_0 = gm_3 \times \frac{(\frac{W}{L})_5}{(\frac{W}{L})_3} \quad (2)$$

$$\tau_1 = \frac{Cgs_3 + Cgs_5}{gm_3} \quad (3)$$

$$\tau_2 = C1(R1+R2) \quad (4)$$

The desired response occurs when the closed-loop poles meet on the real axis; this is true when the condition

$$\frac{\tau_1\tau_2(1+G_0R1)}{(\tau_1+\tau_2)^2} = \frac{1}{4} \quad (5)$$

is met. Note that this condition involves only component ratios; hence the shape of the step response should be insensitive to manufacturing tolerances. At this Q=1/2 condition the pole frequency is

$$\omega_0 = \frac{\tau_1+\tau_2}{2\tau_1\tau_2} = \frac{1}{2\tau_1} \quad (6)$$

The pole frequency is controlled mainly by the g_m/C_{gs} ratio of the NMOS device. This ratio is the most stable naturally-occurring time constant in a CMOS process, since it is nearly unaffected by oxide thickness variations and doesn't depend on NMOS-PMOS tracking. The major source of variation will be L_g which is controlled to better than 10%.

To investigate the tolerance of shaping time to process variations, Monte Carlo SPICE simulations were done. The parameters that were allowed to vary were polysilicon sheet resistance, poly1-poly2 capacitance, and NMOS and PMOS TOX, U0, VFB, CJO, CGSO, CGDO, DW, and DL. All were given uncorrelated Gaussian variations with σ = 15% of mean. Results are shown in Table 3. As expected, peaking time remains stable to within 10% of its mean value. In contrast, a shaper using Sallen-Key lowpass stages and ideal op-amps was also simulated. This design, appropriate for discrete device technology where active device variations are greater than those of passive components, relies on resistor-capacitor products to set the peaking time. Similar R and C variations result in a σ_{tp} of about 18% of the mean.

Finally, Fig. 6 presents the results of simulations of the preamp-shaper combination. Fig. 6(a) shows the input current waveform for a minimum-ionizing particle at normal incidence as generated by GARFIELD[3]. Fig. 6(b) shows the shaper output, which reproduces the major features of the current waveform with the higher frequency components removed by the lowpass filtering.

Fig. 6(c) and (d) show the input and output waveforms for a 45° minimum ionizing particle. Fig. 6(e) and (f) illustrate a 0° MIP with superimposed TR photon; note the change in vertical scale.

3. GARFIELD simulations provided by B. Yu.

In a real system, the long tail of the current waveform would be cancelled by a simple passive pole-zero compensation network which could be on- or off-chip.

4.4 Flash ADC

The resolution, accuracy, and timing goals of the FADC are shown in Table 4. As discussed earlier, the high sampling rate gives position resolution while the amplitude measurement serves to distinguish hadrons from electrons accompanied by a TR photon. In addition, accurate measurement of energy loss in the dE/dx region can improve electron/hadron separation due to the relativistic rise.

A block diagram of the FADC architecture is shown in Fig. 7. The critical subcircuits of the FADC are the input track and hold and the comparators. In the track and hold, high speed must be maintained while clock feedthrough is minimized. Fig. 8 shows three schemes for clock feedthrough cancellation. In the first (Fig. 8a), no cancellation, charge on the switch transistor's CGD and channel charge are injected on the hold capacitor when the switch turns off. In Fig. 8(b) a dummy transistor of 1/2 the width of the switch and clocked in antiphase is placed in series with the switch. Now when CLK goes high, a compensating amount of charge is withdrawn from the storage node. However, this scheme only compensates the CGD of the switch; its channel charge flows unequally due to the unequal impedance seen at its source and drain. Fig 8(c) gives a partial cancellation of this effect by incorporating two dummy switches on either side of the main switch. During turn-off, they present approximately equal impedance on each node.

SPICE circuit simulations illustrating the charge cancellation schemes are shown in Fig. 9. One can see that the first and second order techniques achieve feedthrough cancellation of 92% and 98% respectively.

The proposed latched comparator circuit schematic is shown in Fig. 10[4]. A low-offset voltage differential amplifier is cascaded with a very fast latch to achieve 4-bit resolution with 7-bit accuracy at a 40 MHz sample rate. In the differential amp, transistors have channel lengths 2-3 times minimum. This will minimize offset voltage that results from fluctuations in channel length. Layout is optimized for device matching, that is: same geometry, same orientation, same surroundings, and common-centroid configuration. P-channel input transistors are used to allow input common-mode range near ground with a single 5-V supply. Also, hot carrier instabilities are reduced with P-channel devices.

The latch uses minimum size devices for maximum speed. The preceding amplifier stage eliminates the need to minimize offset voltage in this stage.

The behavior of the latched comparator in simulation is presented in Fig. 11. As shown, a minimum set-up time of 15 nsec is achieved for 20 mV overdrive.

4.5 Analog Pipeline

Many issues at the architecture, circuit, and interface level are involved in a discussion of analog pipeline design and cannot be covered in detail here. A more complete discussion of this work can be found in the reference[5].

The function of the analog pipeline is to minimize the cost and power requirements of ADC systems needing >10 bit resolution, by buffering the encoding process to the Level 1 trigger rate (L1). The time

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4. A. Yukawa, "A CMOS 8-bit High-SPeed A/D Converter IC," IEEE Journal of Solid-State Circuits, 20 (3), 775-779 (1985)
5. W. Sippach, "Analog Pipelines for RHIC," Nevis Laboratories note, Sept. 1991

required to form the L1 trigger determines the length of the analog pipeline. For OASIS, the largest trigger delay is about 1 μs for the liquid argon calorimeter. After the delay, the data from the pipeline can be encoded during an allowed L1 trigger deadtime of about 10 μs. Alternatively, the pipeline data can be derandomized and encoded during the average 100 μs interval between L1 triggers. The latter solution reduces the ADC bandwidth by an order of magnitude, but at the expense of a more complicated analog data-handling process. Extra buffer locations must be added on-chip for holding the data undergoing derandomization, and these locations must be able to hold for a much longer time without loss of signal from low-level leakage currents. If the buffer locations are separate from the locations used for the pipeline delay, then a deadtime must be tolerated during the transfer from pipeline to buffer. If on the other hand the buffer locations are physically commingled with the pipeline cells, then "skip" or "relabel" logic must be used to protect the buffer cells from being overwritten by data entering the pipeline. In this case the read address is not equal to the write address minus a constant offset, so a list of currently-used buffer locations must be maintained and updated each L1 and L2. In addition, the memory may need to be capable of simultaneous read and write and of resolving contention between asynchronously-arriving beam-crossing, L1, and L2 read. write, and relabel requests.

A first test chip is designed to study the switched capacitor cells and readout amplifiers (Fig. 12.) It has 4 channels of 10 independently-addressable cells each. N, P, and CMOS switches are distinguished externally and the folded cascode output amplifier (Fig. 13) can be programmed to measure either voltage or charge. Dual NMOS and PMOS versions are included.

The system is expected to have a noise floor of about 100 microvolts and a linear dynamic range of 3V operating from a 5V supply. The output amplifier has a gain-bandwidth product of about 30 MHz and settles to 0.1% in 250 nsec in simulation.

5.0 Status

A test chip for the TRD/Tracker shaping amplifier has been designed and sent to MOSIS for fabrication in the Orbit 2 μm n-well CMOS process. Completed circuits have been received and initial testing shows performance in close agreement with simulation results. Fig 14 shows an oscilloscope photograph of the step response of the shaper IC. The peaking time is about 75 nsec.

An 8-channel chip, based on the same shaper design but with devices scaled for lower power consumption, is in fabrication now and devices are expected back in late January 1992.

A track and hold and comparator circuit as described in section 4.4 on page 4 is in final layout.

A test chip for the analog pipeline (see section 4.5 on page 5) is in final layout and will be sent to fabrication shortly.

6.0 Summary

A set of CMOS ASICs were developed for the OASIS experiment. In-house ASIC designers participated in the decisions on system partitioning and technology choice during the R&D stage of the detector design. Three functions (Liquid Argon analog pipeline/derandomizer, TRD/Tracker preamp/shaper and flash ADC) were targeted for ASIC development to give the maximum impact of this technology on system performance and cost. A detailed set of baseline specifications were laid out and circuit designs have been completed for the critical subcircuits. Layout and prototyping work has begun and initial results (TRD/Tracker shaping amplifier) are quite promising. These developments are ongoing and will be adapted as necessary to meet future RHIC and/or SSC requirements.

Tables

1. TRD/Tracker charge and current.
2. TRD/Tracker preamp/shaper specifications.
3. Shaper Monte Carlo simulation results.
4. FADC specifications

Figures

1. OASIS detector readout electronics.
2. TRD/Tracker cross section and waveform characteristics.
3. (a) ENC vs. Wg for preamp; (b) ENC vs. Id for preamp.
4. Proposed preamplifier schematic.
5. Proposed shaper schematic.
6. (a),(c),(e) - GARFIELD simulations of TRD/Tracker anode current waveforms for MIP at 0°, 45°, and 0° MIP + TR photon; (b),(d),(f) - preamp/shaper output (simulated).
7. FADC block diagram.
8. Track and hold clock feedthrough cancellation schemes.
9. Track and hold clock feedthrough simulations.
10. Comparator circuit.
11. Comparator simulations.
12. Analog memory test chip.
13. Folded cascode output amplifier for analog memory test chip.
14. Oscilloscope photograph of CMOS shaping amp - vertical, 500 mV/div, horizontal, 50 nsec/div.

TABLE 1. TRD/Tracker charge and current.

	MIP	TR	Total	Unit
Anode current	1.3	7-33	1.3-3.4	uA
Duration	0.2 - 1.5	~.07	•	usec
Charge	0.3 - 2.0	0.5 - 2.4	0.3 - 4.4	pC

TABLE 2. TRD/Tracker preamp/shaper specifications.

Channels/chip	4-8
ENC	2500 e- rms
Shaping function	Unipolar, semi-Gaussian impulse response
Peak time	70 nsec
FWHM	<100 nsec
Pole-zero cancellation	For detector tail and preamp feedback pole
Outputs	X1, X10 (for TR, MIP resp.) 2 V full scale

TABLE 3. *Shaper Monte Carlo simulation results.*

Quantity	Mean	St. Dev.	St.Dev./Mean(%)	Units
Step Response Peaking Time	81.1	8.14	10	nsec
DC Gain	1.0	.21		21

TABLE 4. FADC Specifications

ADCs per chip	4-8
Resolution	4 bit
Accuracy	1% of full scale
Sample Rate	40 MHz
Input bandwidth	20 MHz
Power	<100 mW/ADC

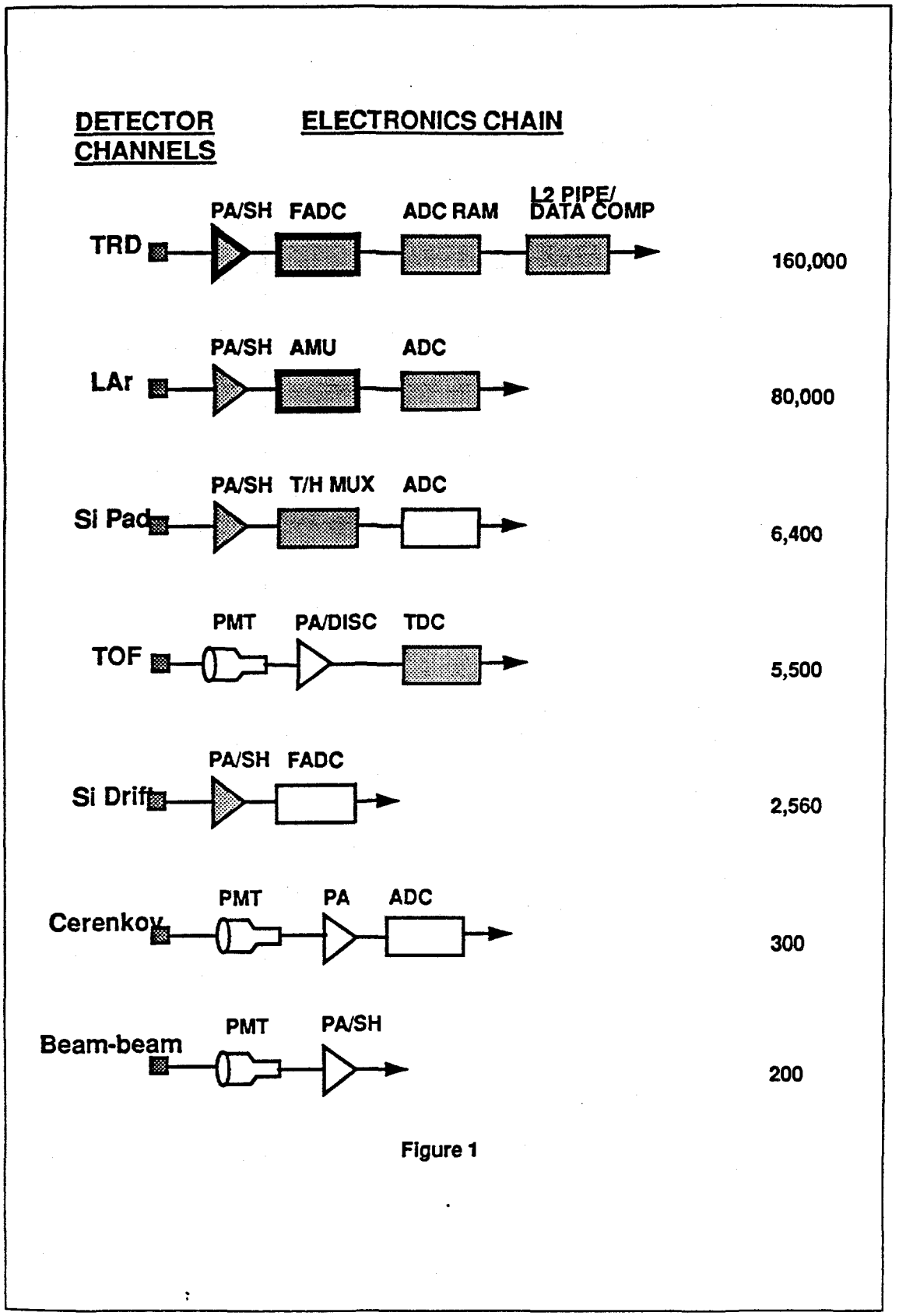

DETECTOR CHANNELS
ELECTRONICS CHAIN
TRD
PA/SH
FADC
ADC RAM
L2 PIPE/ DATA COMP
160,000
LAr
PA/SH
AMU
ADC
80,000
Si Pad
PA/SH
T/H MUX
ADC
6,400
TOF
PMT
PA/DISC
TDC
5,500
Si Drift
PA/SH
FADC
2,560
Cerenkov
PMT
PA
ADC
300
Beam-beam
PMT
PA/SH
200

Figure 1

TRD Detector and Signal Characteristics

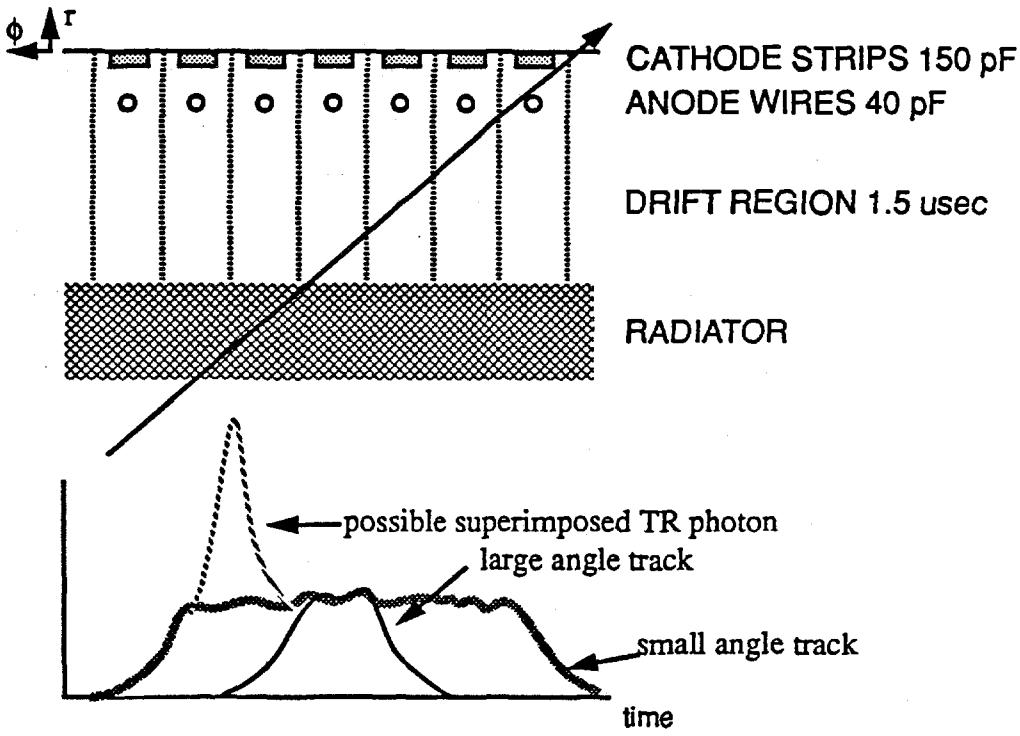


Fig. 2

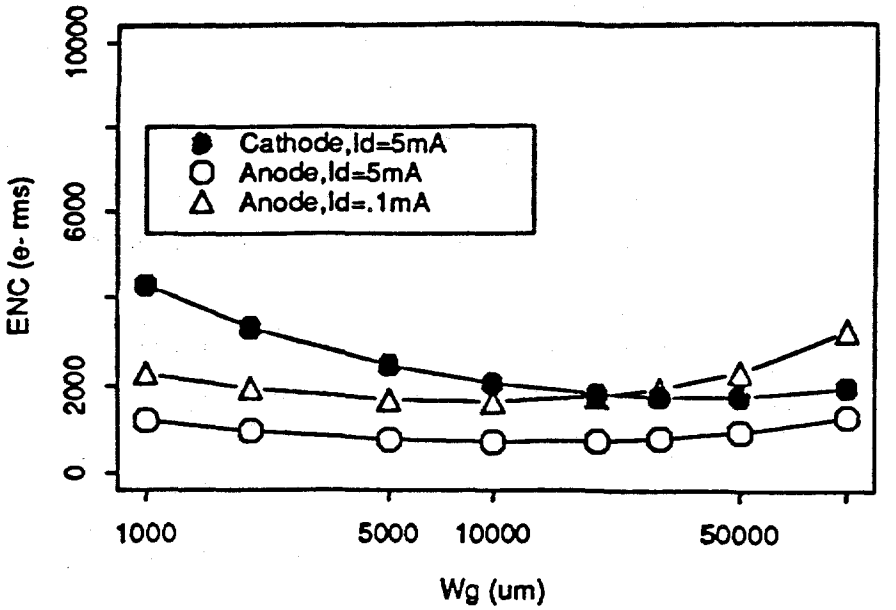


Figure 3(a)

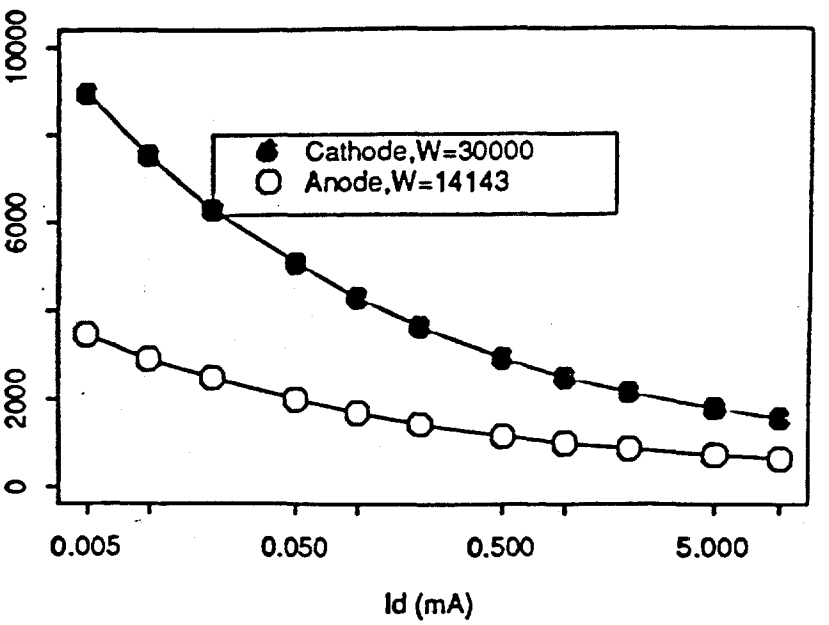
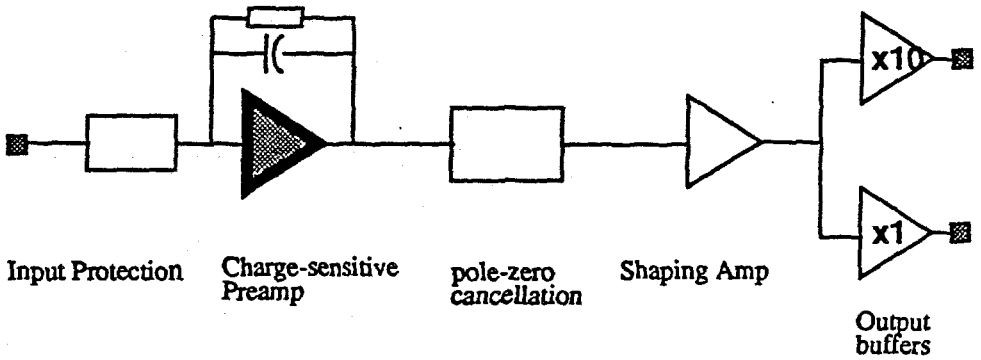


Figure 3(b)

PREAMP/SHAPER



Preamp

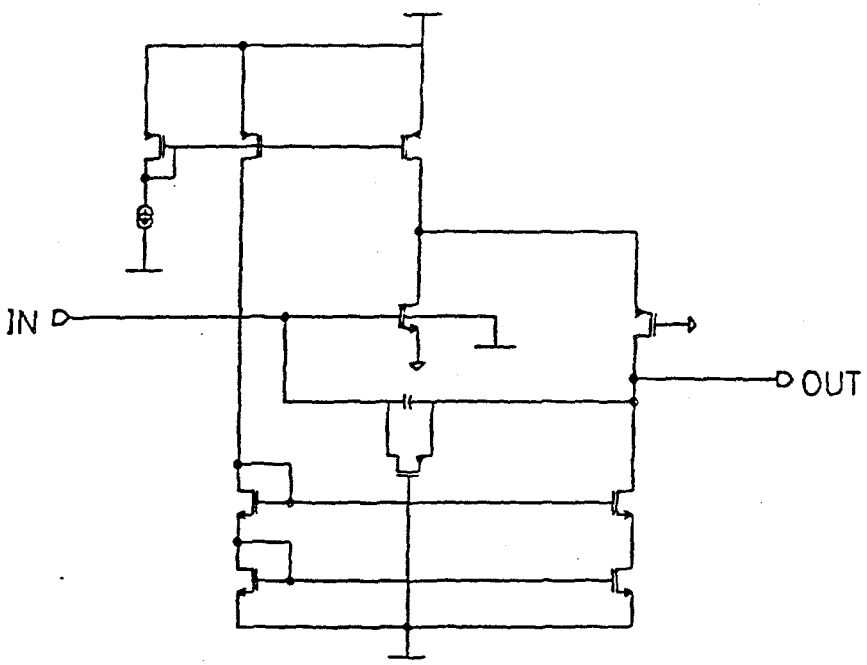
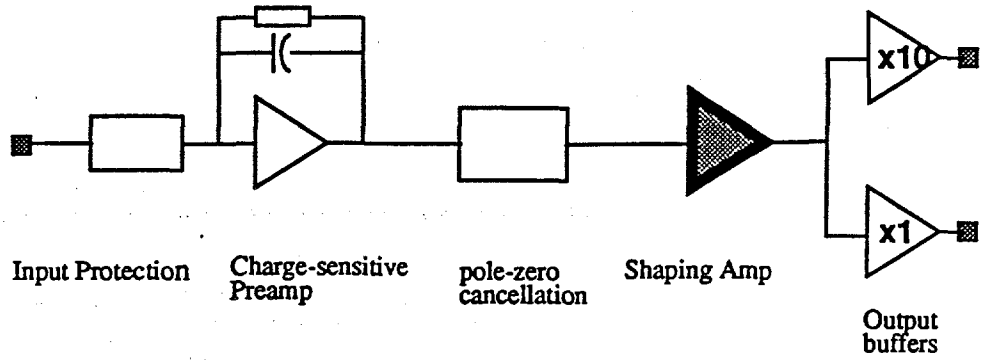


Figure 4

PREAMP/SHAPER



Shaping Amp - Lowpass Section

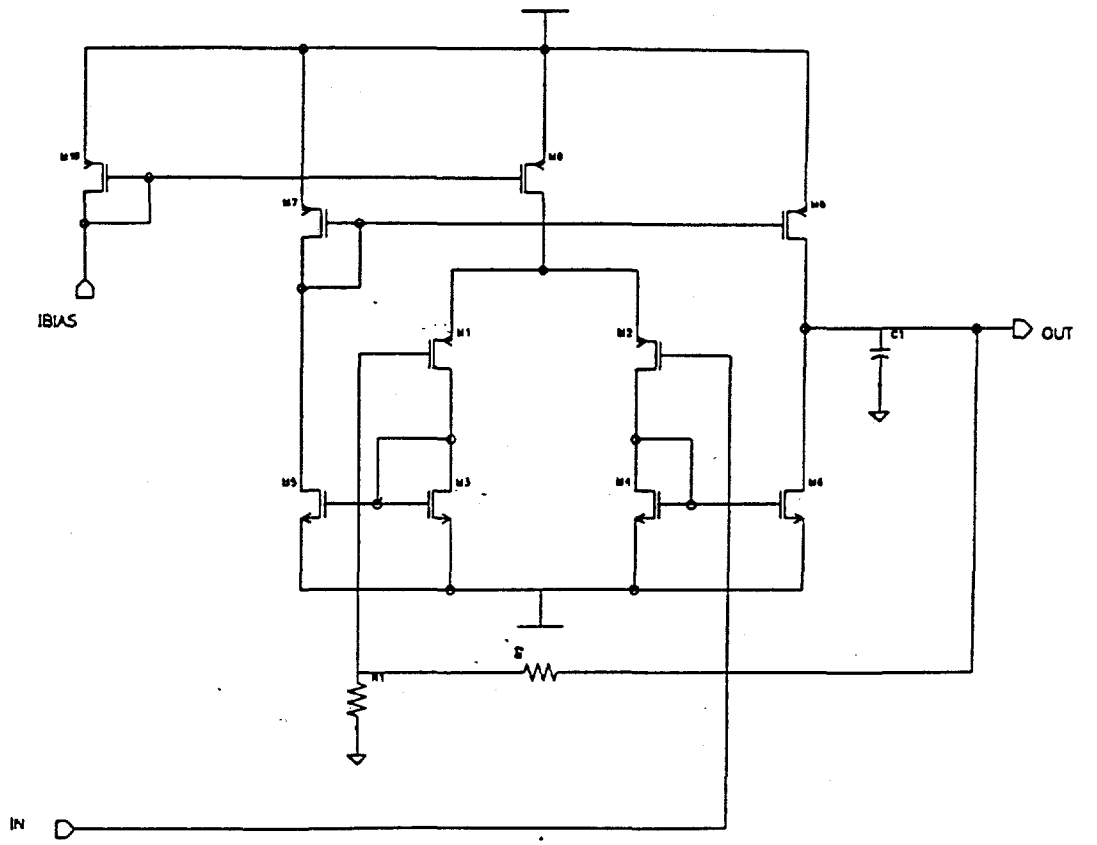


Figure 5

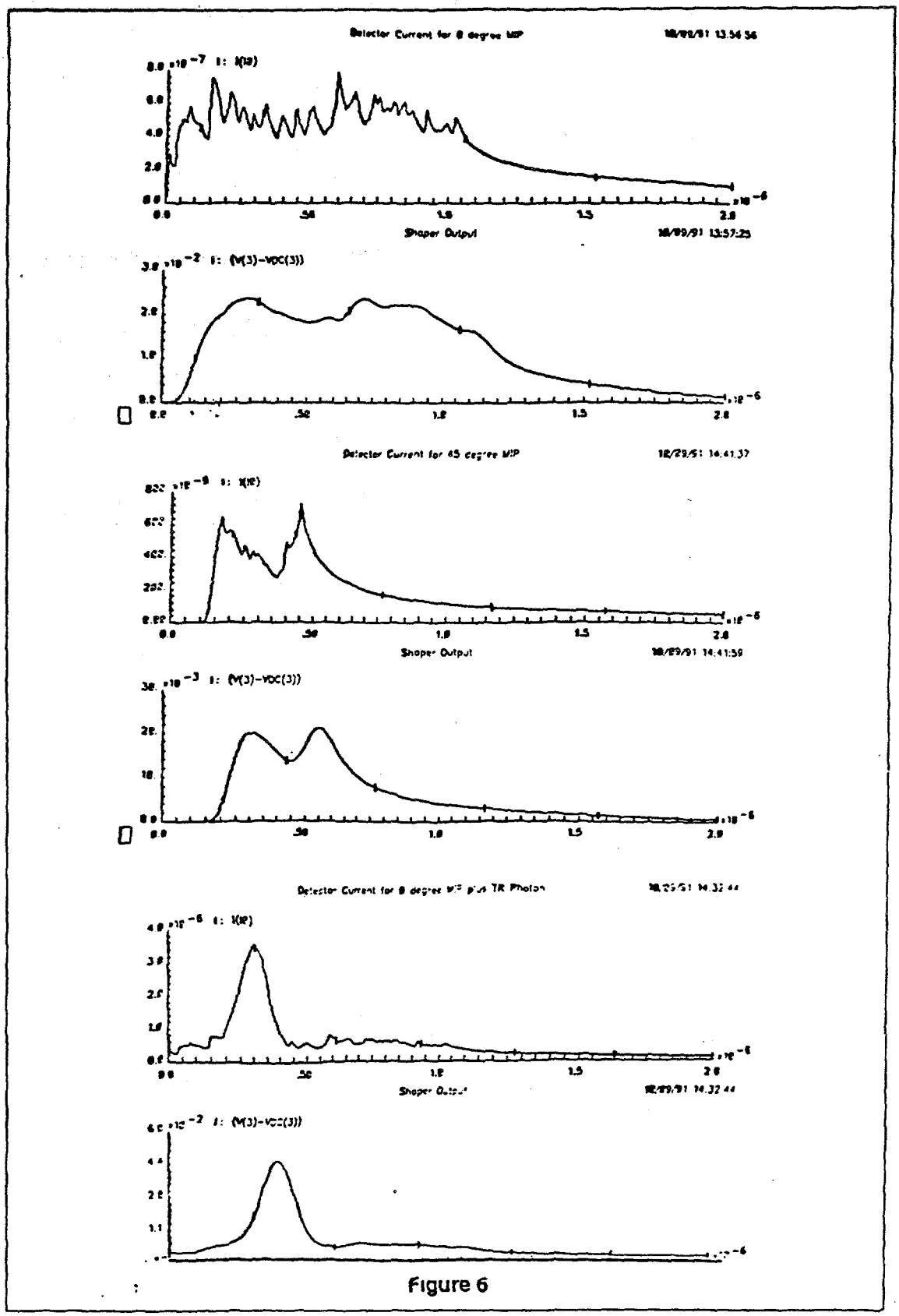
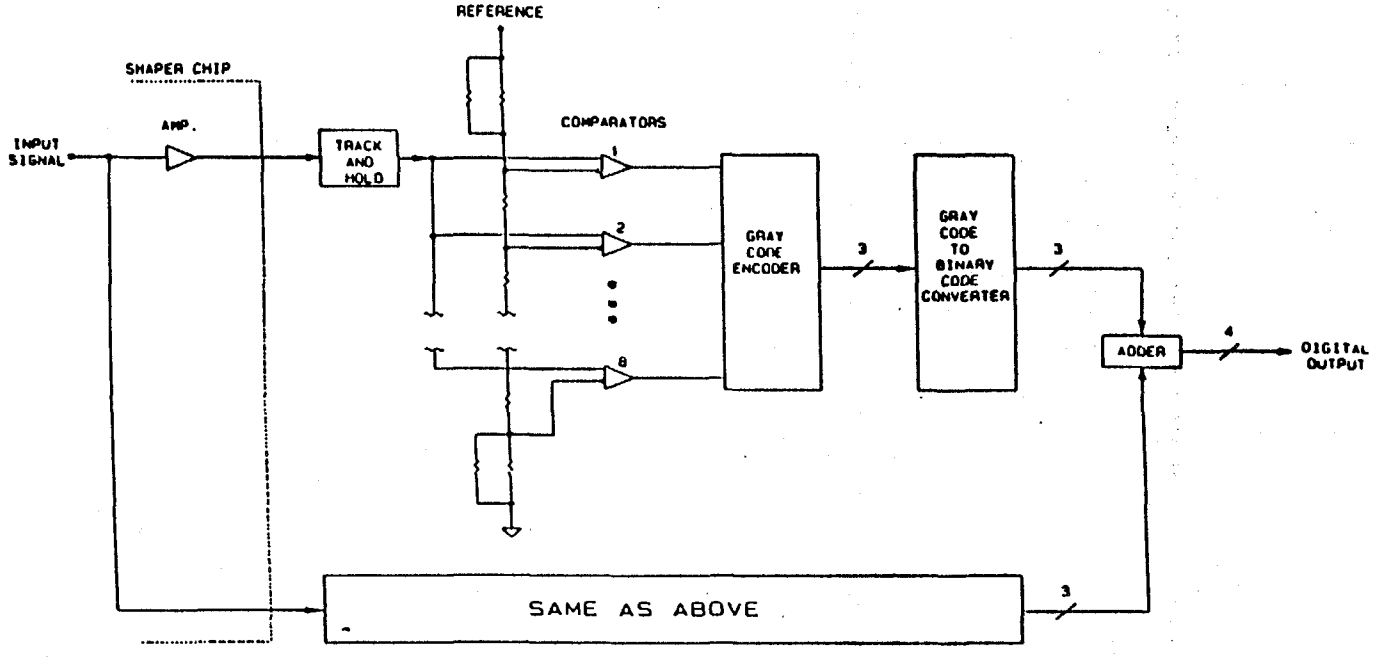

Detector Current for 0 degree MIP
I: I(0)
Shaper Output
I: (V(3)-VDC(3))
Detector Current for 45 degree MIP
I: I(0)
Shaper Output
I: (V(3)-VDC(3))
Detector Current for 0 degree MIP plus TR Photon
I: I(0)
Shaper Output
I: (V(3)-VDC(3))

Figure 6



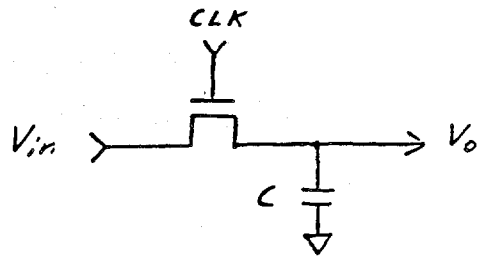
Overall architecture of the proposed ADC. The input signal is divided into high and low level components by the preceeding shaper chip. This is done to keep low level analog signals away from the noisy ADC chip and also to reduce the offset voltage requirement for the comparators. Two similar 3-bit ADC's are used to produce a 4-bit output.

Figure 7

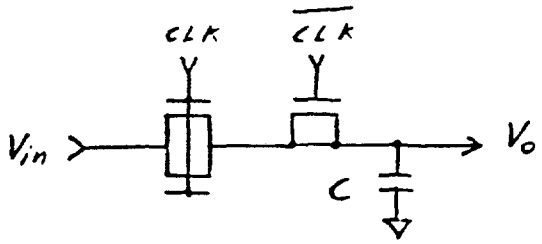
CRITICAL SUBCIRCUITS

TRACK AND HOLD —— High speed must be maintained with minimal clock feedthrough.

a) No charge cancellation



b) First order charge cancellation



c) Second order charge cancellation

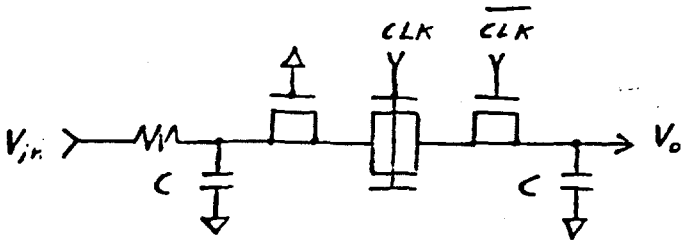
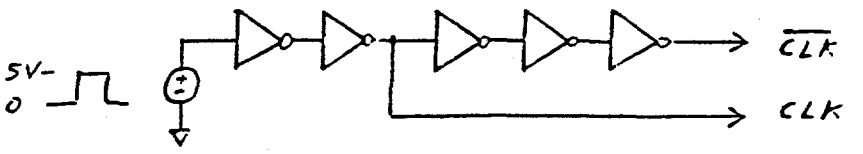


Figure 8

SIMULATIONS

- BSIM1 MOS models are used with parameter values supplied from a ORBIT 2 micron analog run.
- W/L = 3/2 (minimum geometry)
- C = 0.5 pF
- CLK is obtained as follows:



a) No charge cancellation

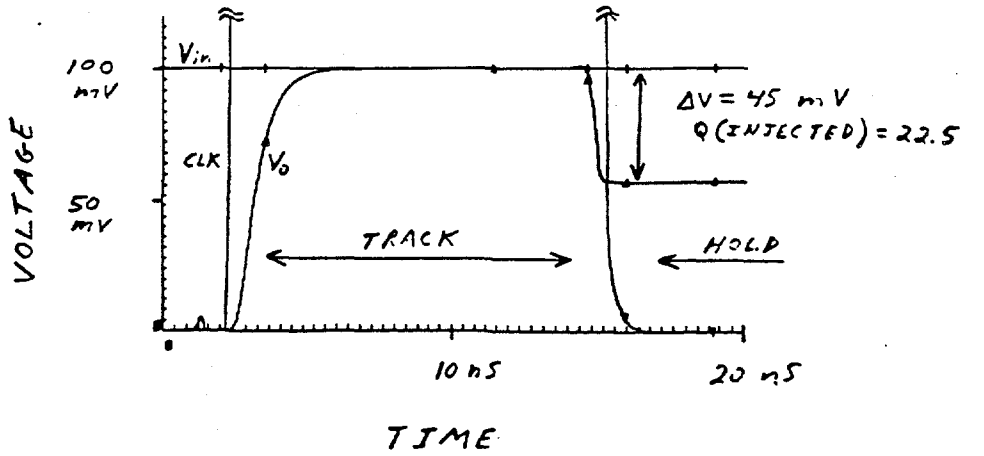
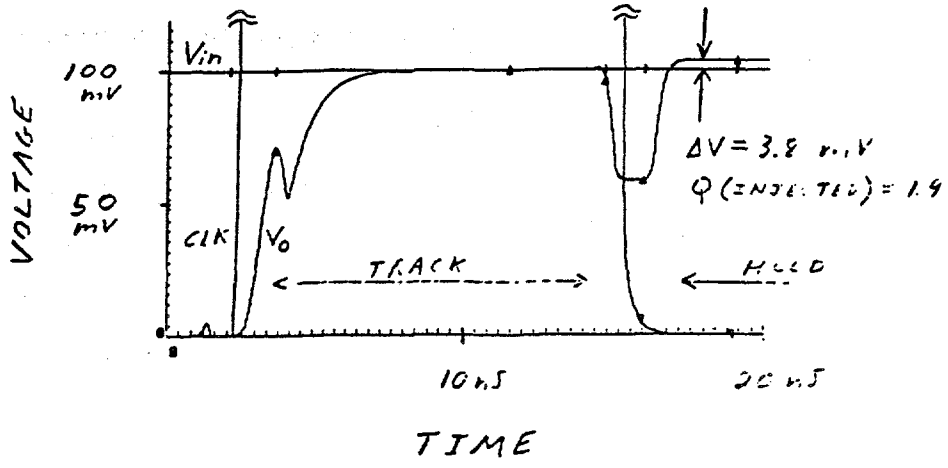


Figure 9

b) **First order charge canellation**



c) **Second order charge cancellation**

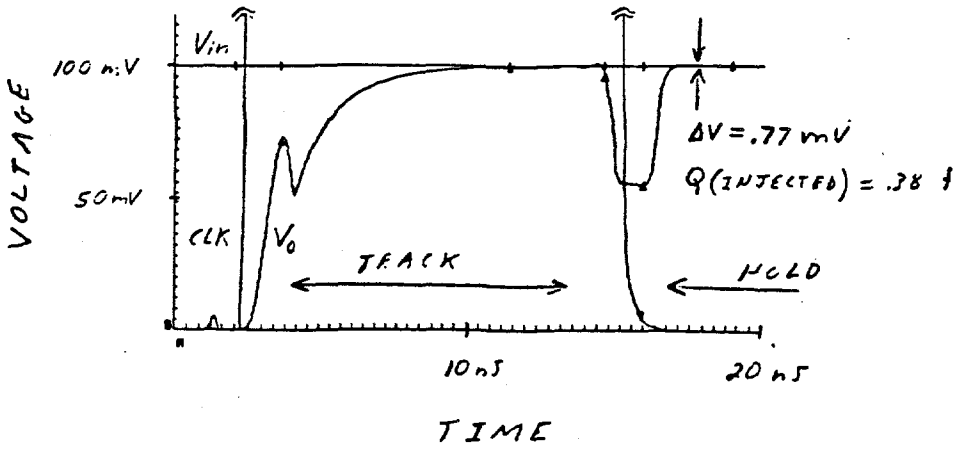


Figure 9

LATCHED COMPARATOR

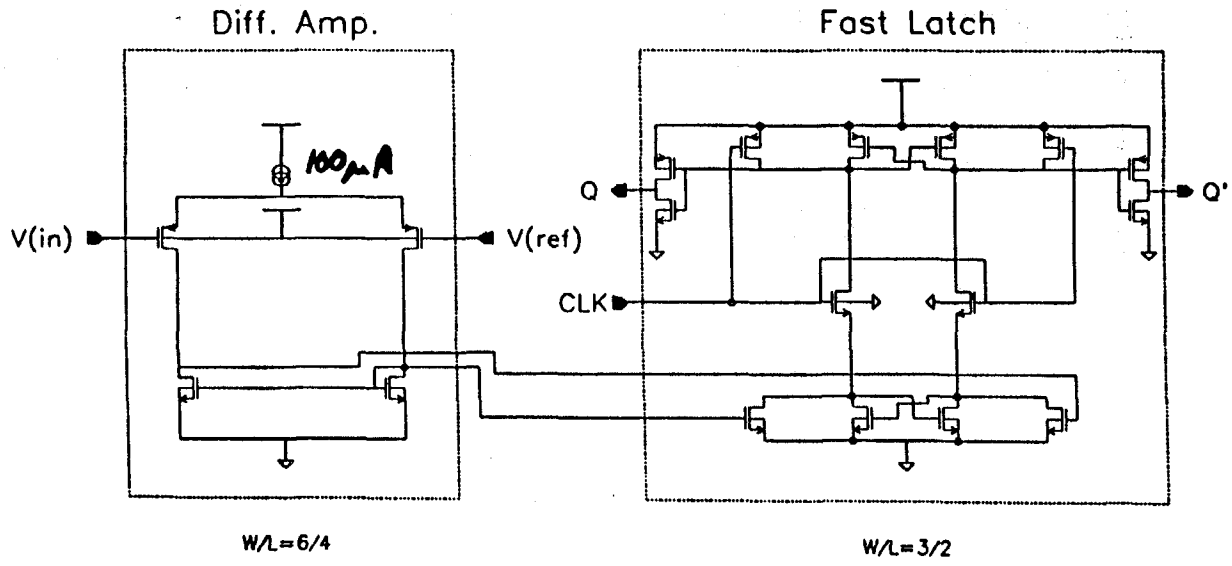


Figure 10

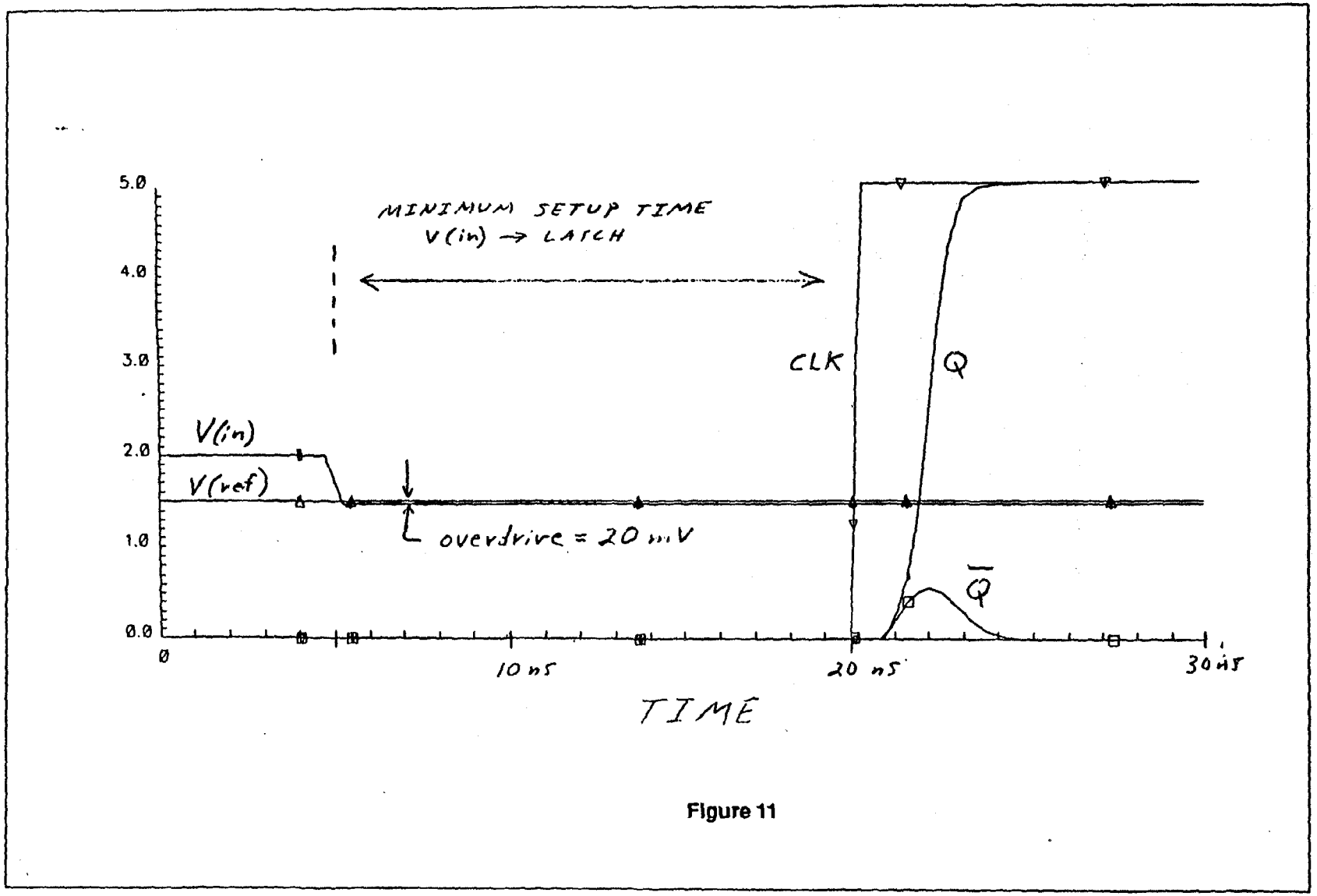

5.0
4.0
3.0
2.0
1.0
0.0
0
10 nS
20 nS
30 nS
TIME
MINIMUM SETUP TIME
V(in) → LATCH
CLK
Q
$\overline{Q}$
V(in)
V(ref)
overdrive = 20 mV

Figure 11

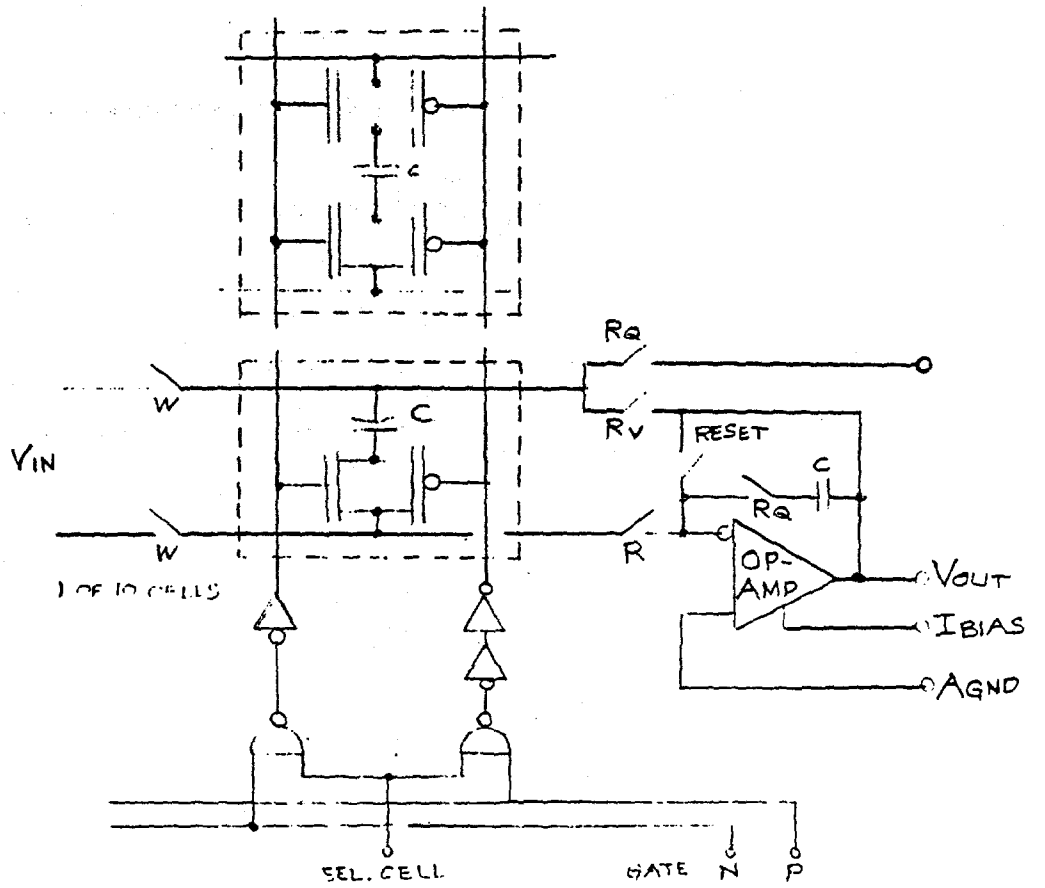

C
RQ
W
C
RV
RESET
VIN
C
RQ
W
R
OP-
AMP
VOUT
IBIAS
AGND
SEL. CELL
GATE
N
P

Figure 12

FOLDED CASCODE OP-AMP

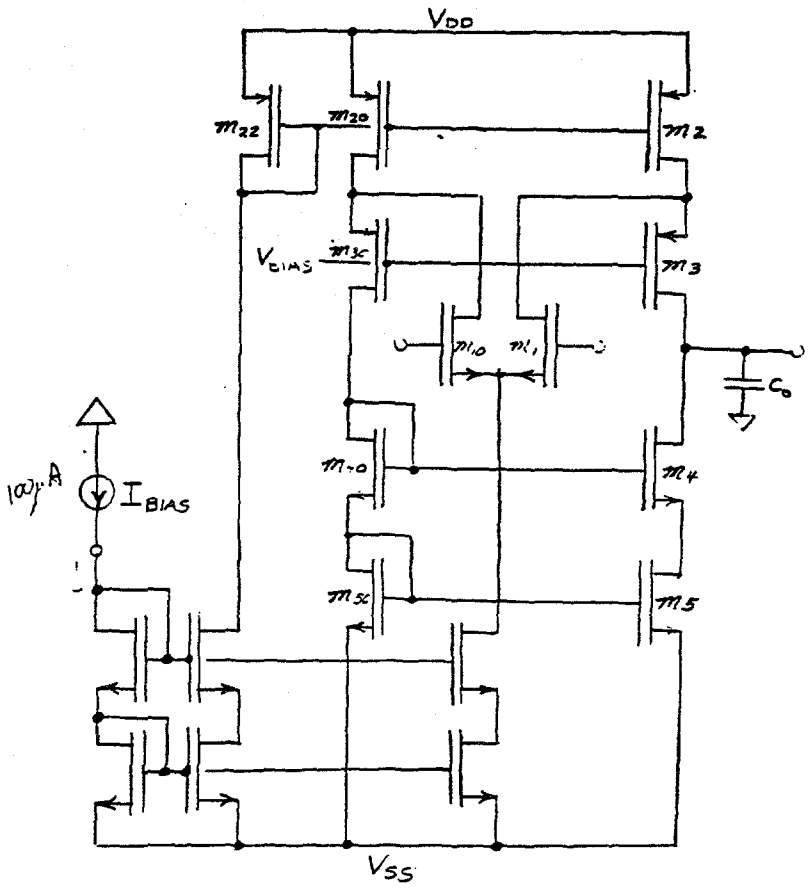


Figure 13

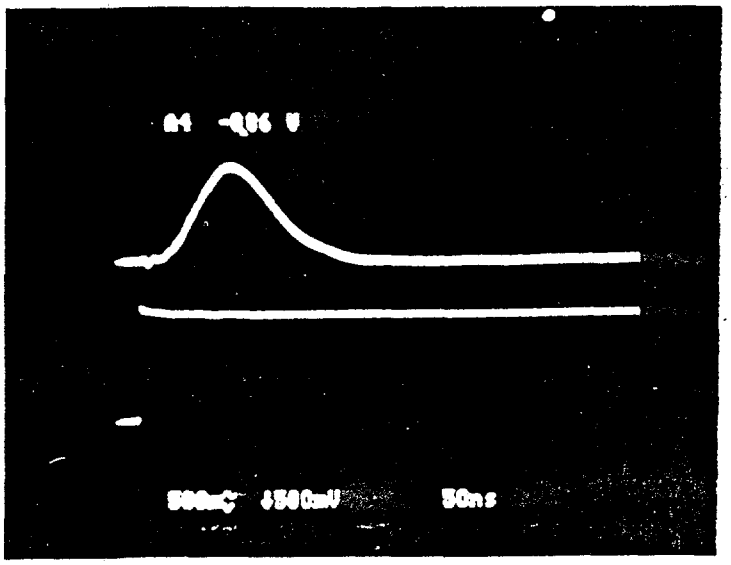


Figure 14

DISCLAIMER