THERMOSONIC WIRE BONDING OF IC DEVICES USING PALLADIUM WIRE

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ABSTRACT

The feasibility of replacing gold wire by palladium wire in thermosonic wire bonding of CMOS and bipolar devices are studied in terms of the manufacturability, physical, electrical and assembly performance. The results show that palladium wire is a viable option for bonding the bipolar devices but not the CMOS devices.

INTRODUCTION

The current practice of using gold wire in thermosonic bonding of IC devices in the semiconductor manufacturing industries is costly. If gold wire can be replaced by palladium wire in bonding, the production cost of IC can be reduced.

Palladium is chosen in the study because being a group VIII element, it has chemical and physical properties quite similar to those of the gold. It has f_{cc} crystal structure like gold and is readily fabricated at room temperature. However, palladium is harder compared to gold and has a tensile strength of 200 Mpa. Its coefficient of linear expansion is smaller, resistivity higher and thermal conductivity lower compared to gold. Although palladium has the disadvantage of forming an oxide film at temperature greater than 400°C and has a poor resistance to highly oxidizing environments, these two properties have little effect on its usability as a thermosonic bonding wire of the IC.

The present study investigated the feasibility of replacing gold wire by palladium wire in thermosonic wire bonding of IC in terms of the manufacturability, physical, electrical and assembly performance.

EXPERIMENTAL

The experiments were carried out using a bipolar and two different CMOS devices. For each type of devices, group P were thermosonically bonded using palladium wire whilst group G which acted as the control were thermosonically bonded using gold wire. The bonding machine used is Shinkawa type UTC-50.

The bond pads of the two CMOS devices (CMOS1 and CMOS2) are of similar structure and materials. It comprises of an Al layer on top of the vapox on the silicon substrate. For the bipolar devices, there is an extra layer of hard TiW in between the Al and vapox layers. The CMOS1 and the bipolar devices have 22 leads per lead frame while CMOS2 devices have 20 leads per lead frame. Similar lead frames and mold compound were used for all the devices. The diameter of the palladium and gold wires used were 1.3 mil.

The thermosonically bonded IC devices that underwent bond pull and ball shear tests were not molded. Five units of each of these wire-bonded devices were randomly chosen to undergo simulated post-mold cure. In the simulated post-mold cure, the unmolded devices were heated at 200°C for 2 hours before undergoing ball shear test. Another five units of these devices were also randomly selected to undergo nickel decoration to check for cratering phenomenon to ensure that the bonding force and power used were not excessive.

Those wire-bonded devices that were molded subsequently underwent the usual post-mold curing, marking, trimming and forming processes before being subjected to X-ray inspection for wire deflection and non-sticking-on pad (NSOP)[1]. The molded units that were cross-sectioned for intermetallic formation inspection were stressed by high temperature storage (HTS) at 200°C for 168, 336 and 500 hours. Those molded units that were subjected

to electrical functional test were stressed for 168, 336 and 500 hours by operating life test (OPL). The functional test was carried out to ensure the correct logical function of the device and that all the processing defects were found. As the VOL test which is used to assure the input threshold levels of the devices is easily affected by the voltage drop, this functional test was carried out to compare the resistivity of the palladium wire with that of the gold wire.

RESULTS AND DISCUSSION

Table 1 shows the average pull strength obtained for the three different devices. In general, devices with palladium wires have stronger bond pull values compared to those with gold wires. This is as expected since palladium is stronger than gold and has higher Young modulus. The differences in the bond pull strengths between the palladium and gold wires in both the CMOS devices, are however, not significant. Only in the bipolar devices, the palladium wire average bond pull strength is significantly higher than the gold wire average bond pull strength.

Column two of Table 2 shows the ball shear results for the three different devices without simulated post-mold cure at 200°C for 2 hours. Both CMOS devices with gold wire have higher ball shear values compared with those of palladium wire. When the SEM photographs of the palladium ball bond formed (photo 1a) was inspected, it was found that they were more spherical compared to those of the gold ball bond formed (photo 1b) for both the CMOS devices. The more spherical shape implied a smaller contact surface between the palladium ball and the bond pad since the palladium is harder than gold. This explains why the ball shear value of the palladium ball in the CMOS devices being lower. For the bipolar devices, the ball shear value for the palladium ball is higher compared to that of the gold ball. The SEM photos show the bipolar palladium and gold ball bonds formed are more similar in shape (photos 2a and 2b).

Column three of Table 2 shows the average ball shear strength obtained after the unmolded devices were heated for 2 hours at 200°C. For palladium ball bonds, the ball shear strengths remained very much the same as those without the heat treatment. The gold ball bonds for all the devices on the contrary showed a clear rise in the ball shear strength after the heat treatment. The heat treatment had strengthened the gold ball bond. The intermetallic cross-section study helped elucidating these results. For all the three devices with gold wire ball bond, Au-Al intermetallic formation was observed at zero hour time point (photo 3a). As the HTS time point increased, the intermetallic layer became thicker (photo 3b) thus increasing the bond strength [2]. For all the three devices with the palladium wire bonding, the Pd-Al intermetallic formation was not observed until 336 hours of HTS stress at 200°C (photo 4). The growth of intermetallic layer follows Kidson equation[3],

$$X = C \exp(-E/KT)\, t^{0.5}$$

where E is the activation energy and t is the time interval.

Since the activation energy of palladium and gold are 63.6 kcal/mol and 27 kcal/mol respectively, it explained why Pd-Al intermetallics growth is slower than that of Au-Al intermetallics. The slower growth rate of Pd-Al intermetallic is less likely to cause Kirkendall voids [3] failure under higher HTS time point. Nonetheless up till 1000 hours time point HTS, no void was detected for all the devices bonded either with palladium or gold.

The bond pull and ball shear results thus showed that palladium wire is not a good substitute of the gold wire in the thermosonic bonding of the CMOS devices. Furthermore, the photos of the intermetallic cross-section of all the palladium ball bond (photo 4) showed that there was a `spark-like' diffusion of the palladium into the surrounding mold compound starting at 168 hours time out. In the case of the gold ball bond, the gold diffusion into the surrounding mold compound was observed only at 1000 hours time out. All the devices that underwent nickel decoration test did not show cratering phenomenon indicating that the bonding force and power used in the study were satisfactory and not excessive.

The X-ray inspection of the molded devices showed that rejects only occurred in the CMOS1P and CMOS2P devices. The CMOS devices do not have the TiW layer in the pad and their rejects were almost all NSOP. The number of rejects out of a total of 200 units inspected for the CMOS1P and CMOS2P devices were 108 and 96 respectively. These results further supported the ball shear test which showed weaker palladium bond formed for the CMOS devices. The harder palladium wire required a stiff TiW layer in the bond pad to prevent the bond pad from cracking during wire bonding. The absence of the TiW layer on the pad caused the palladium bond not well-formed which subsequently triggered NSOP to manifest during the molding process. No reject was observed for CMOS devices that were bonded with gold wire and bipolar devices that were bonded with either gold or palladium wire.

To assess the degree of wire sweep, the wire deflection was observed at two positions using the X-ray. The first position was at the wire bonded at the corner of the lead frame at an angle of ~45° to the direction of flow of the mold compound whilst the second position was at the wire bonded perpendicular to the direction of flow of the mold compound. The wire deflection W, was measured by $W = 100\frac{Y}{X}$ where X is the distance between the first and second bond and Y is the maximum height of the wire loop. Table 3 shows the wire deflection results obtained at these two positions. For CMOS1 devices, the palladium wires had deflected more than the gold wires. For CMOS2 and bipolar devices, the difference in the wire deflection between the palladium and gold wires were not so significant. Palladium being harder than gold requires slightly longer length for the same bonding in order to reduce stress in the wire looping profile. Longer wire length is more likely to sweep during molding process and also to cause sagging defect. However, owing to the bigger die size of the CMOS2 and bipolar devices, shorter wires were required for bonding the die to the lead frame. This explained why wire deflection was not critical when palladium wires were used for bonding in these devices.

The functional VOL tests results for all the devices bonded either with palladium or gold wires were not affected by the OPL within 500 hours time point. Table 4 shows the average VOL voltage obtained for the devices under the OPL stress. The production specification voltages for the CMOS1, CMOS2 and bipolar devices are 0.36V, 0.26V and 0.55V respectively. Although the VOL values obtained for all the devices bonded with palladium wire were higher than those bonded with gold wire because of palladiums higher resistivity, they are still way within the production specification values.

CONCLUSION

The manufacturability of the bipolar devices bonded with palladium wire is 96% and comparable to that of the gold wire (97%). Its assembly ability and physical performance (pull strength, ball shear strength, ball formation and wire sweep) using palladium wires are also comparable if not better than those using gold wire. In spite of palladium's higher resistivity, the bipolar devices bonded with palladium wire passed the electrical functional test. The two CMOS devices bonded with palladium wires yielded unsatisfactory results in both the physical and electrical tests and their manufacturability were also rather low (44% and 50% respectively). Thus, palladium wire is a viable option for thermosonically bonding the bipolar devices but not the CMOS devices.

REFERENCES

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2 G. Magni, C. Nobile, G. Ottaviani, M. Costato and E. Galli, "Gold-Aluminium Thin Film Interactions and Compound Formation", J. Appl. Phys., Vol. 52, pp. 4047-4054, 1981.

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Table 1: The average pull strengths of the devices bonded with gold or palladium wires.

Devices	Average pull strength (g)
CMOS1G	12.90 ± 1.63
CMOS1P	14.28 ± 2.40
CMOS2G	11.84 ± 1.84
CMOS2P	12.36 ± 2.10
Bipolar G	11.42 ± 1.78
Bipolar P	15.11 ± 2.31

Table 2: The average ball shear strength of the bonded devices without and with simulated post-mold cure at 200°C for 2 hours.

Devices	Average strength (g) without simulated post-mold cure	Average strength (g) with simulated post-mold cure
CMOS1G	58.91 ± 4.15	67.70 ± 6.21
CMOS1P	37.69 ± 5.07	36.94 ± 4.40
CMOS2G	58.27 ± 6.04	77.33 ± 9.99
CMOS2P	34.10 ± 4.99	34.94 ± 4.13
Bipolar G	47.77 ± 5.47	59.91 ± 5.10
Bipolar P	51.05 ± 6.92	50.60 ± 5.57

Table 3: The wire deflection at position 1 and position 2 of the bonded die.

Devices	Position 1	Position 2
CMOS1G	1.98 ± 0.79	1.50 ± 1.03
CMOS1P	5.02 ± 2.51	4.34 ± 2.24
CMOS2G	1.70 ± 0.57	2.84 ± 1.22
CMOS2P	2.34 ± 0.67	4.38 ± 2.54
Bipolar G	2.34 ± 0.88	2.42 ± 0.92
Bipolar P	2.60 ± 1.11	3.50 ± 1.57

Table 4: The average VOL voltage of the bonded devices.

Devices	Average voltage (V)
CMOS1G	0.163
CMOS1P	0.179
CMOS2G	0.159
CMOS2P	0.188
Bipolar G	0.367
Bipolar P	0.382

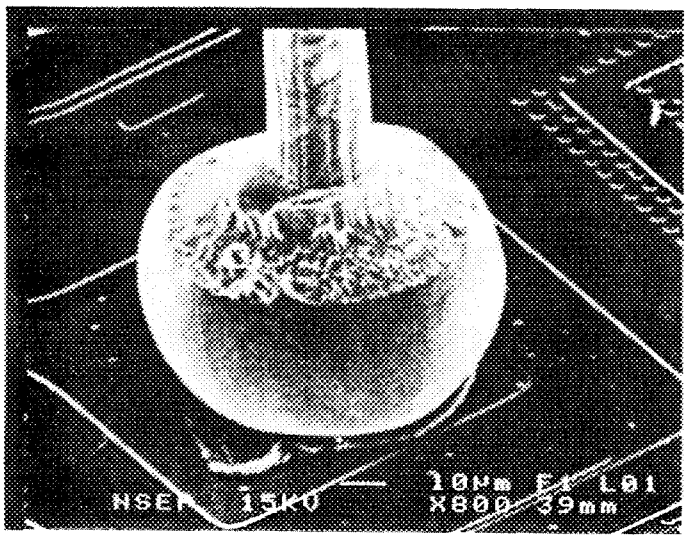

Photo 1a: Palladium ball bond of CMOS device.

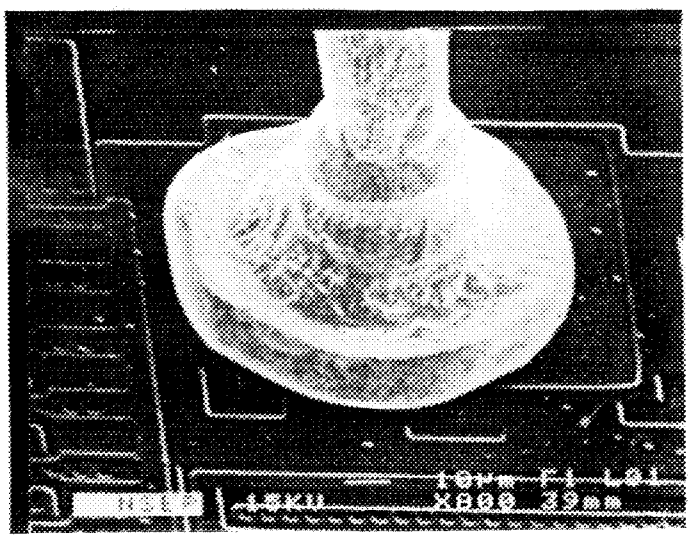

Photo 1b: Gold ball bond of CMOS device.

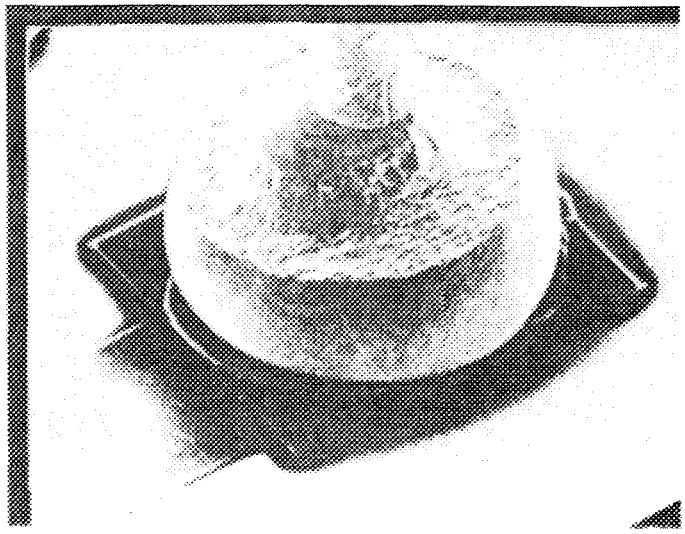

Photo 2a: Palladium ball bond of bipolar device.

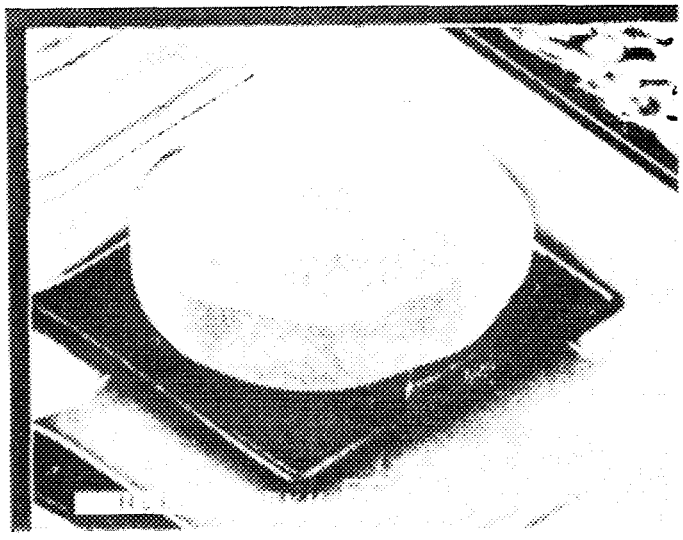

Photo 2b: Gold ball bond of bipolar device.

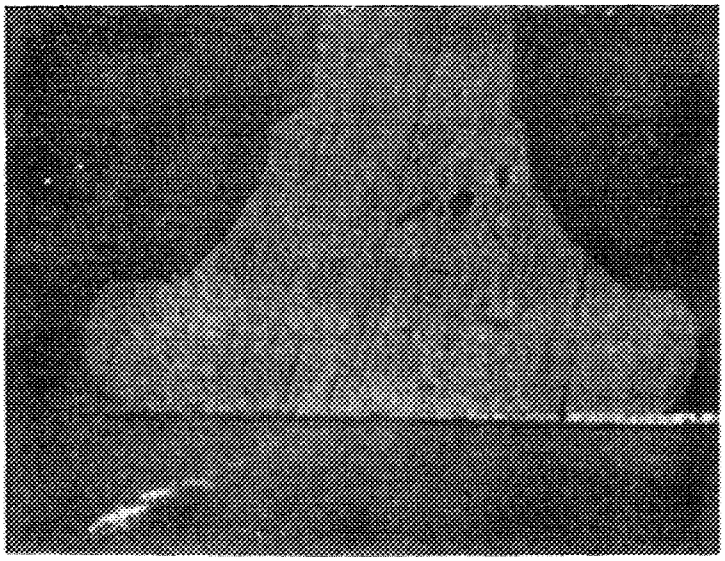

Photo 3a: Au-Al intermetallic formation of CMOS at zero hour.

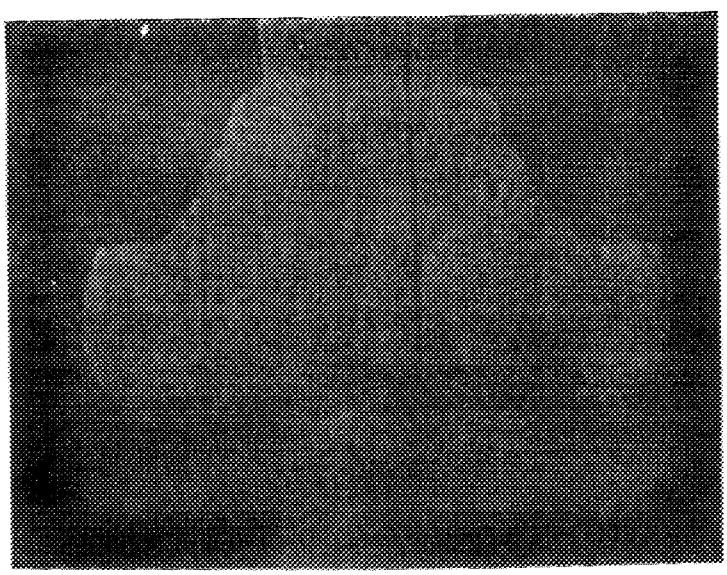

Photo 3b: Au-Al intermetallic formation of CMOS after 336 hours of HTS stress at 200°C.

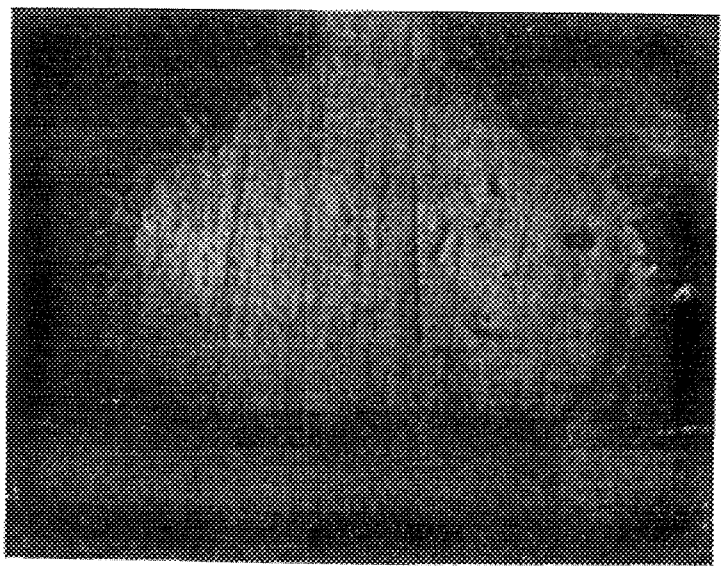

Photo 4: Pd-Al intermetallic formation of CMOS after 336 hours of HTS stress at 200°C.