High density microelectronics package using low temperature cofirable ceramics

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Low Temperature Cofired Ceramics (LTCC) is a relative new thick film process and has many engineering and manufacturing advantages over both the sequential thick film process and high temperature cofired ceramic modules. Because of low firing temperature, low sheet resistance metal conductors, commercial thick film resistors, and thick film capacitors can be buried in or printed on the substrates. A 3-D multilayer ceramic substrate can be prepared via laminating and co-firing process. The packing density of the LTCC substrates can be increased by this 3-D packing technology.

At Kaohsiung Polytechnic Institute (KPI), a LTCC substrate system has been developed for high density packaging applications, which had buried surface capacitors and resistors. The developed cordierite-glass ceramic substrate, which has similar thermal expansion as silicon chip, is a promising material for microelectronic packaging. When the substrates were sintered at temperatures between 850~900 °C, a relative density higher than 96% can be obtained. The substrate had a dielectric constant between 5.5 and 6.5. Ruthenium-based resistor pastes were used for resistors purposes. The resistors fabricated in/on the LTCC substrates were strongly depended on the microstructures developed in the resistor films. Surface resistors were laser trimmed in order to obtain specific values for the resistors.

Material with composition $Pb(Fe_{2/3}W_{1/3})_x(Fe_{1/2}Nb_{1/2})_yTi_2O_3$ was used as dielectric material of the capacitor in the substrate. The material can be sintered at temperatures between 850~930 °C, and has dielectric constant as high as 26000. After cofiring, good adhesion between dieelectric and substrate layers was obtained. Combing the buried resistors and capacitors together with the lamination of LTCC layer, a 3-dimensional multilayered ceramic package was fabricated.

High Density Microelectronics Package Using Low Temperature Cofirable Ceramics

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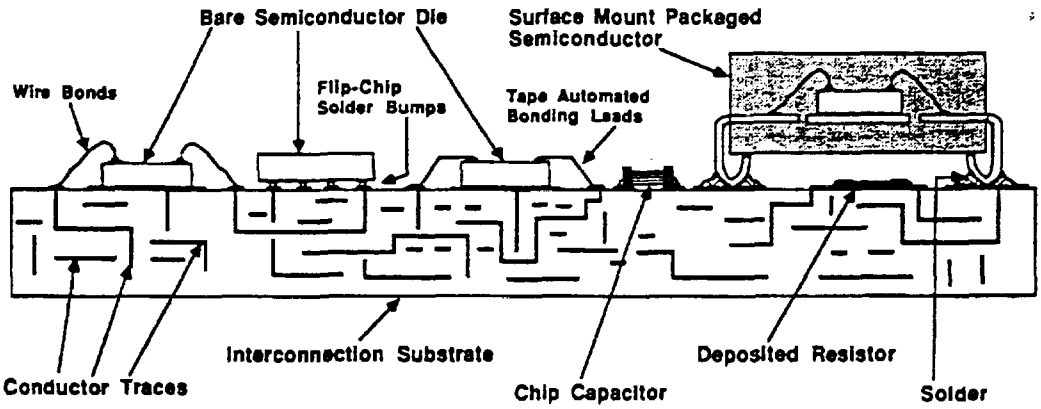
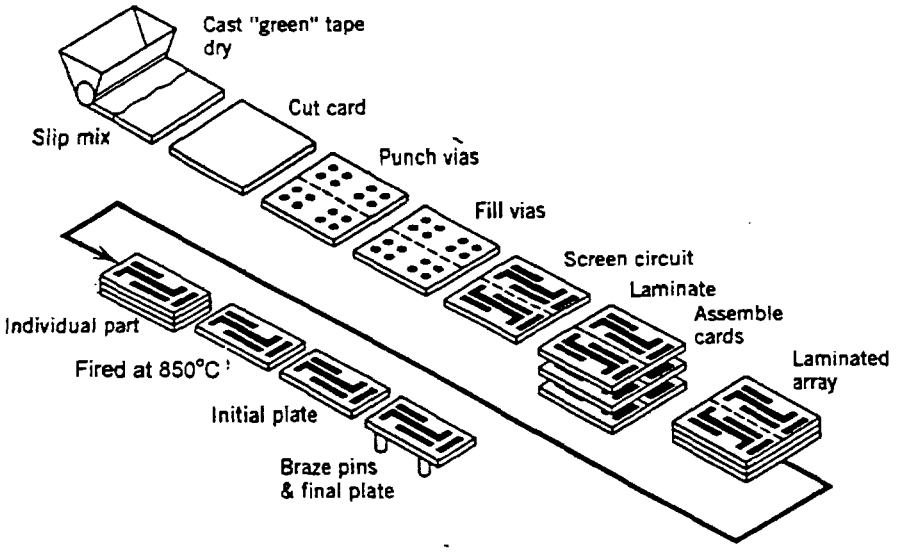
Vienna, Austrian
June, 1997



Cross Section Illustrating Hybrid Microelectronics Technology

Comparison of Characteristic Difference of Multilayer Technology [Vitriol]

MULTILAYRER THICK FILM	LTCC	HTCC
• Requires a mechanical support base • Serial processing • 6 prints per layer (3 dielectric, 2 via fill, 1 conductor) • 60 sequential firing steps for up to 10 layer • Must protect devices	• Monolithic structure • Parallel processing • 2 prints per layer (1 via fill, 1 conductor) • 1 cofire step plus three postfire steps • Hermetic package	
	• Fired at 850°C • Use standard thick film conductors • Fires in air • Tailorable dielectrics	• Fired at 1600°C • Requires refractory metals • Fires in hydrogen • Long processing time to remove organics • Uses alumina dielectric



Fabrication Process of LTCC Substrate

Advantages of the Low Temperature Cofirable Ceramics(LTCC):

1. easy to be laminated and to form multilayer structure,
2. small package area,
3. passive components can be buried in the substrates,
4. via hole can be as small as 0.1mm,
5. high heat dissipation,
6. thermal expansion matches with Si chips.

Researches Related to the Low Temperature Cofirable Ceramics at "***KPI***"

1. Thermal Placement
   -Circuit Routing, Thermal Management.

2. Substrate Materials
   -Cordierite + Borosilicate Glass, Alumina Nitride + Borosilicate Glass.

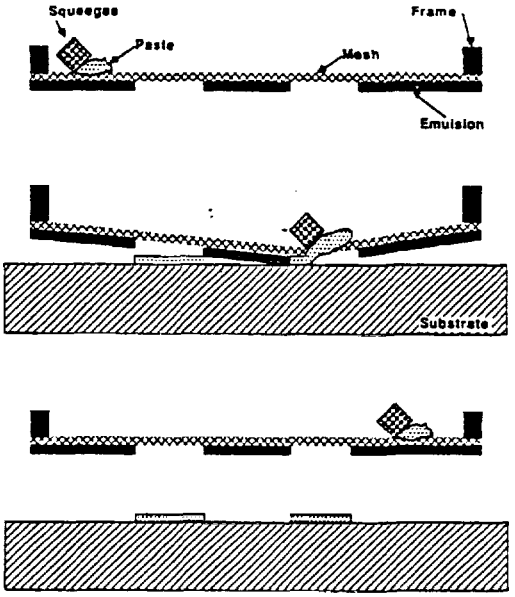
3. Resistor Materials
   -Ruthium Based Resistor,Surface and Buried Resistors, Resistor Trimming.

4. Capactor materials
   -Low Temperature (<950°C) Firable Capacitor, Surface and Buried Capacitors.

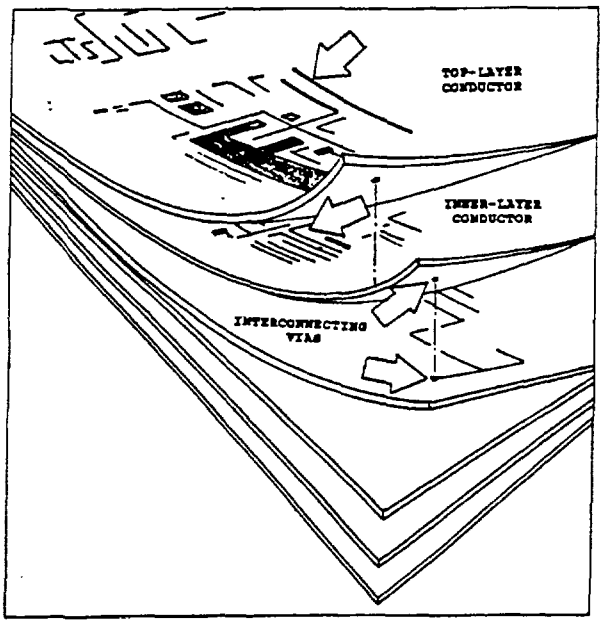
5. Conducting Materials
   -Metallization on the LTCC Substrates, Ball Grid Array.

Process Sequence for Low Temperature Cofirable Ceramic Substrate

Cordierite + Glass Ceramic Green Tape



Screen Printing Process for Material Deposition onto a Substrate



Exploded View of Cofired Ceramic Structure

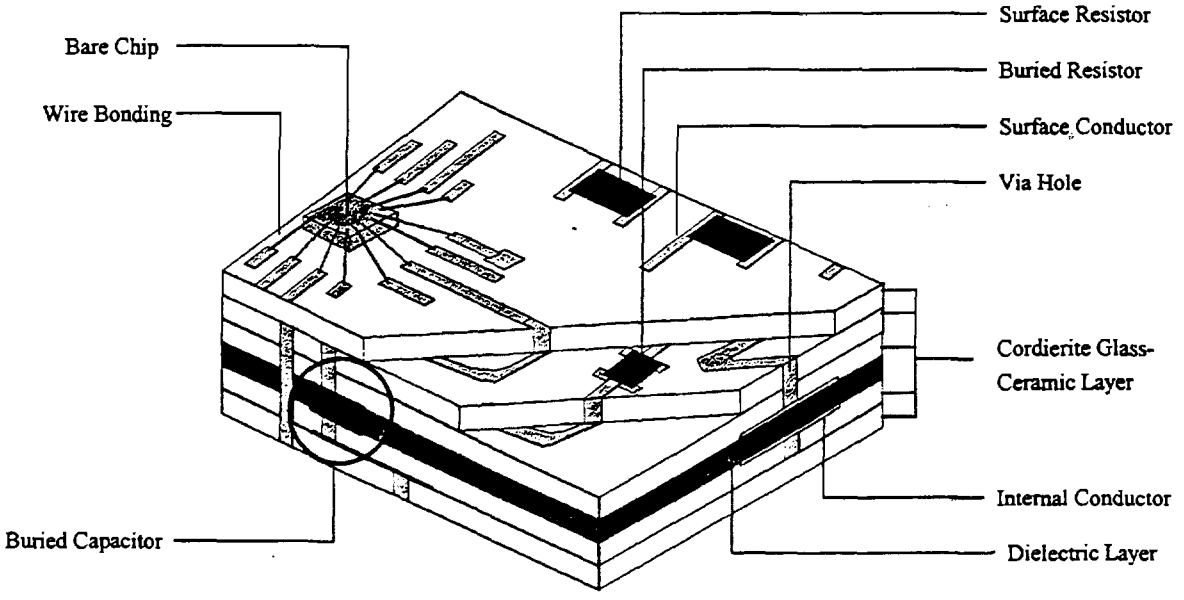
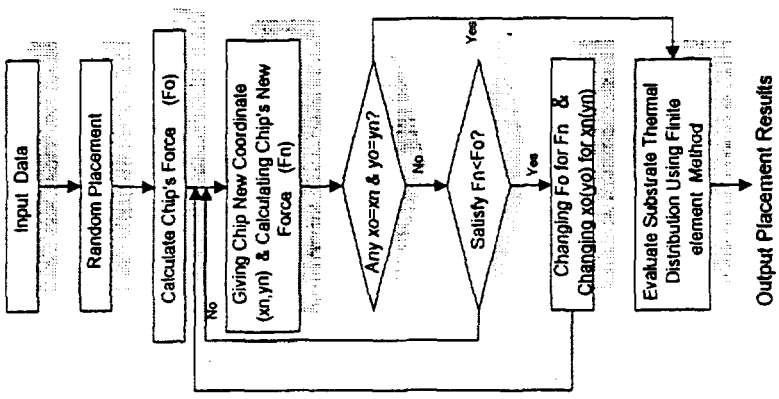
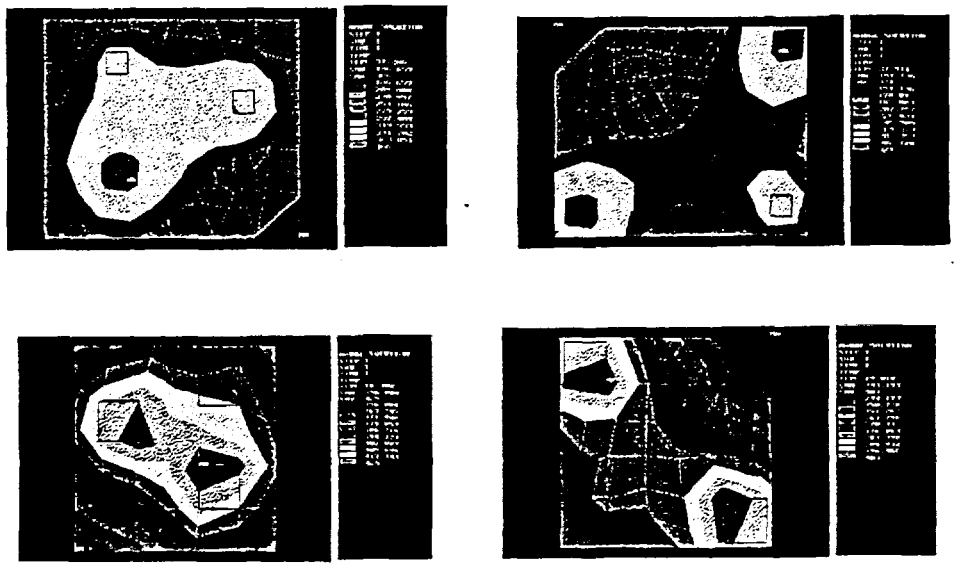


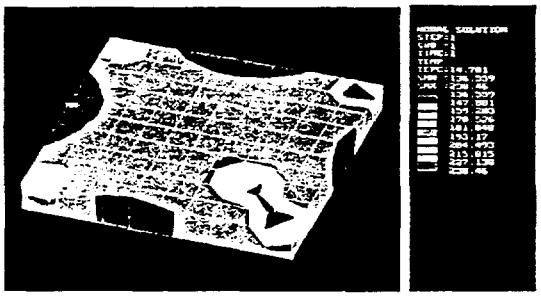
Illustration of Low Temperature Cofirable Ceramic Packaging.

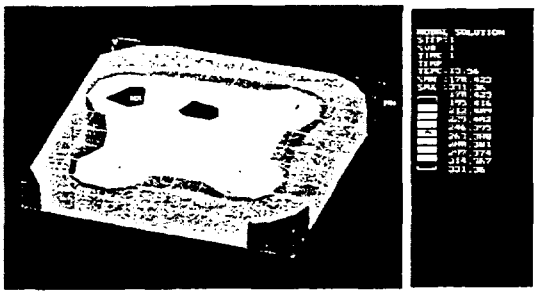




Simulation of Thermal Placement of LTCC Package

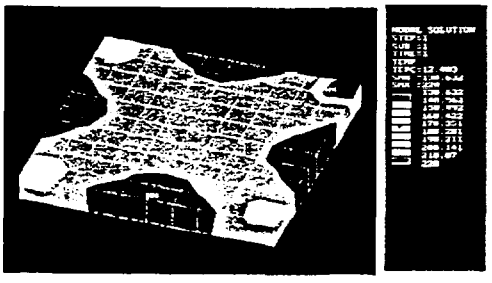
Simulation Results (Case 2)

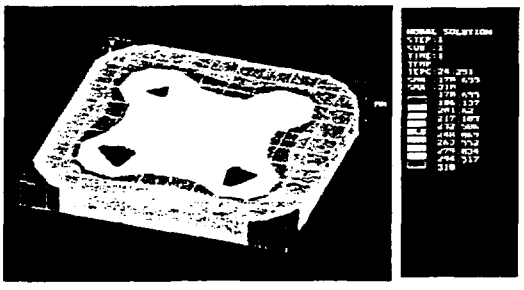




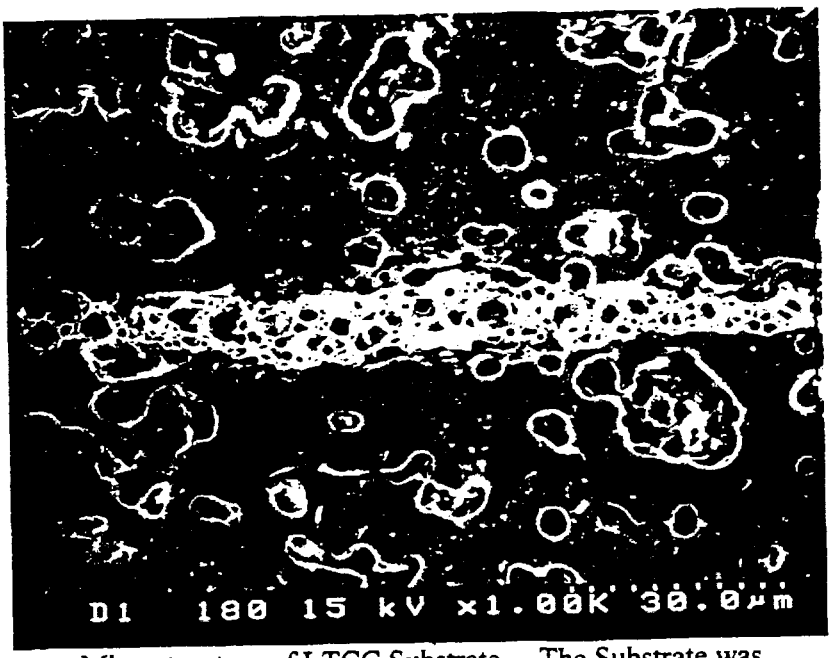
	Quadrisection	FFD
The lowest temperature	178.42°F (81.34°C)	136.56°F (58.09°C)
The highest temperature	331.36°F (166.31°C)	238.46°F (114.70°C)
Max temperature difference	152.94°F (84.97°C)	101.90°F (56.61°C)

Simulation Results (Case 1)

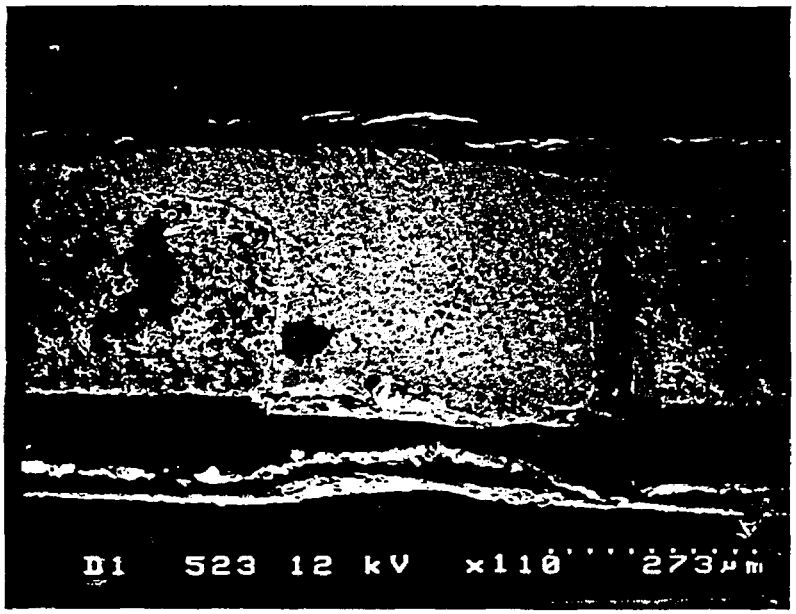




	Quadrisection	FFD
The lowest temperature	170.66°F (77.03°C)	130.63°F (54.79°C)
The highest temperature	310.00°F (154.44°C)	220.00°F (104.44°C)
Max temperature difference	139.34°F (77.41°C)	89.37°F (49.65°C)

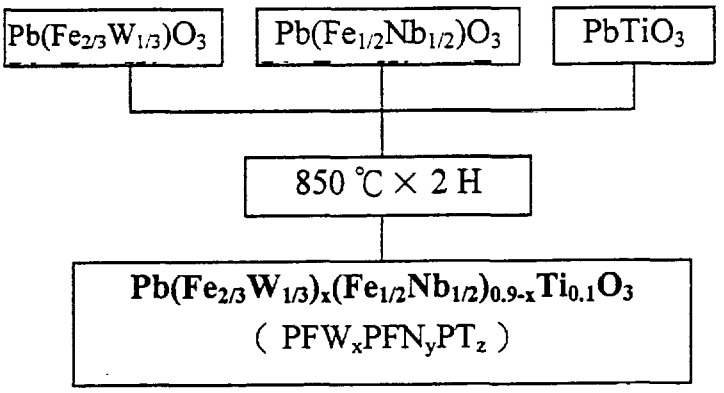


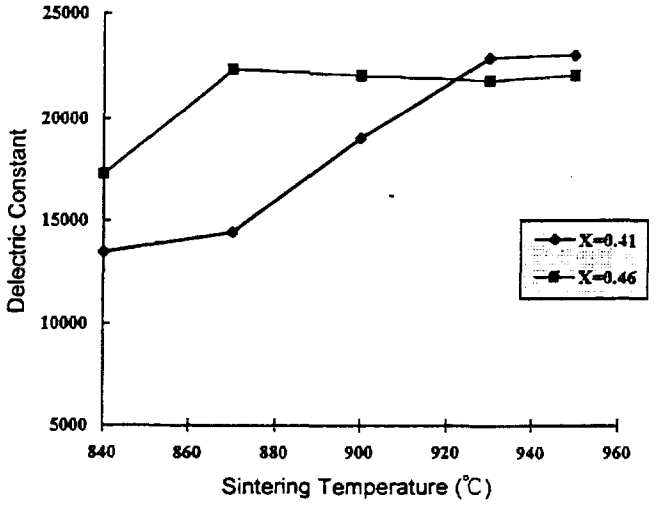
Microstructure of LTCC Substrate. The Substrate was Fired at 850°C for 30 Minutes.



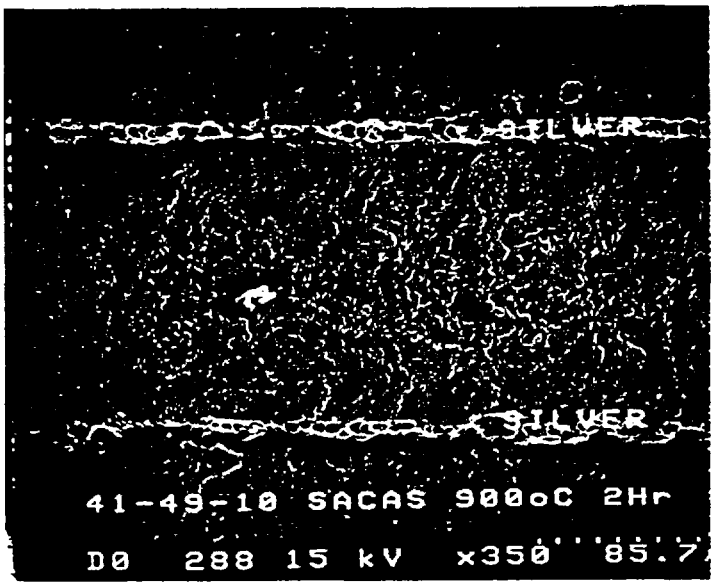
Microstructure of Via Hole through the LTCC Substrate.

Calcination of $Pb(Fe_{2/3}W_{1/3})_x(Fe_{1/2}Nb_{1/2})_{0.9-x}Ti_{0.1}O_3$

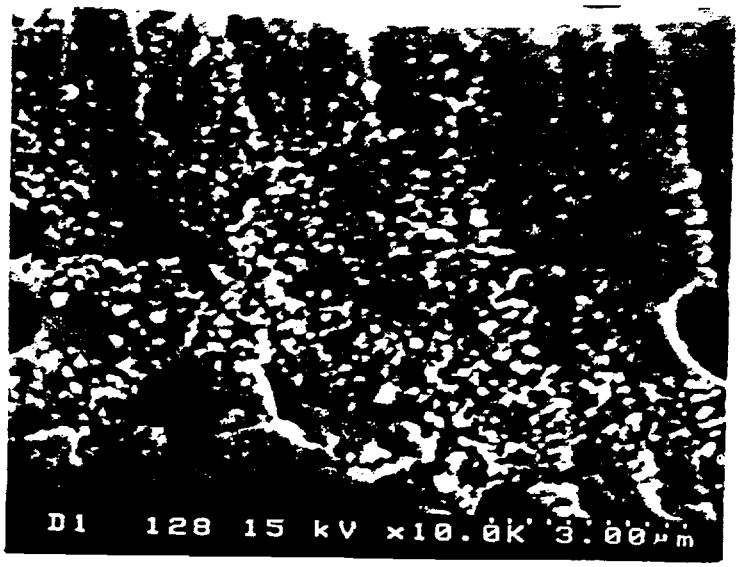




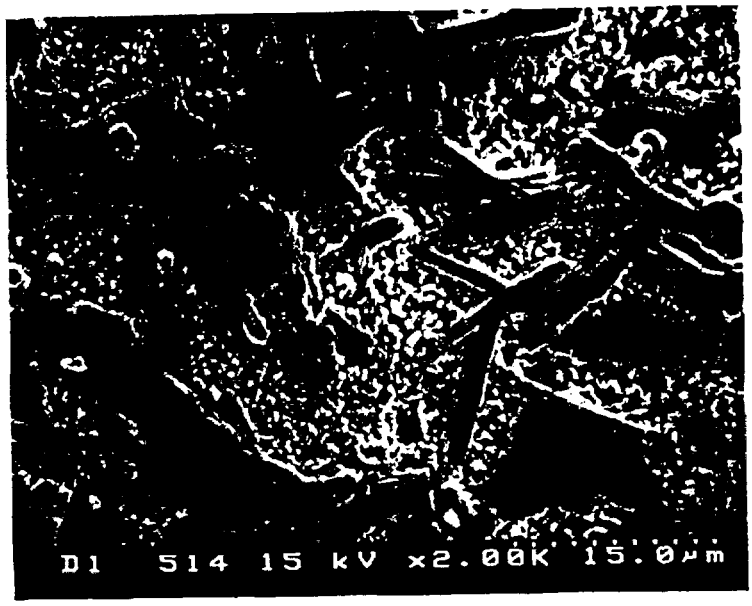
Effect of sintering temperature on the dielectric constants of $PFW_xPFN_{0.9-x}PT_{0.1}$ relaxors ,the sintering time is 1 hour.



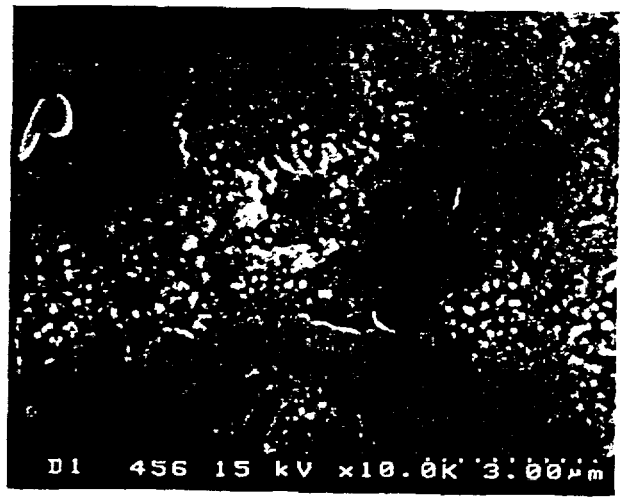
Microstructure of Buried Capacitor in the LTCC Substrate



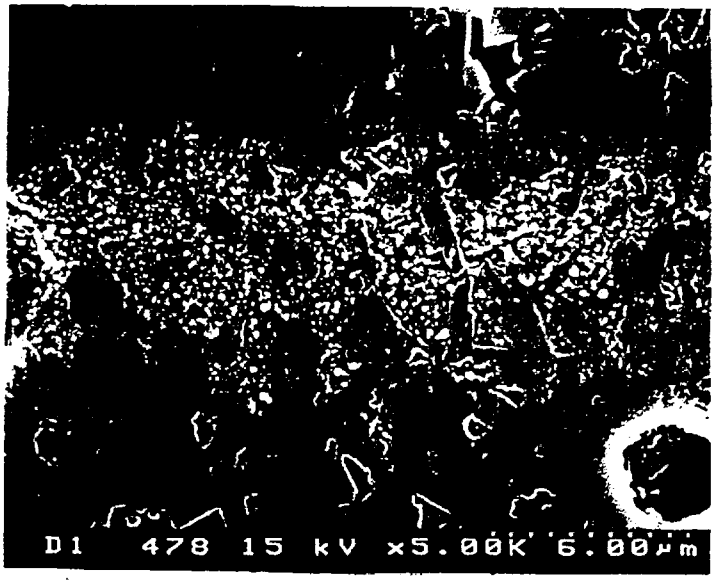
Cross-section of Shoei 1kΩ Resistor printed of the Alumina Substrate.
The Sample was Fired at 850°C for 30 Minutes.



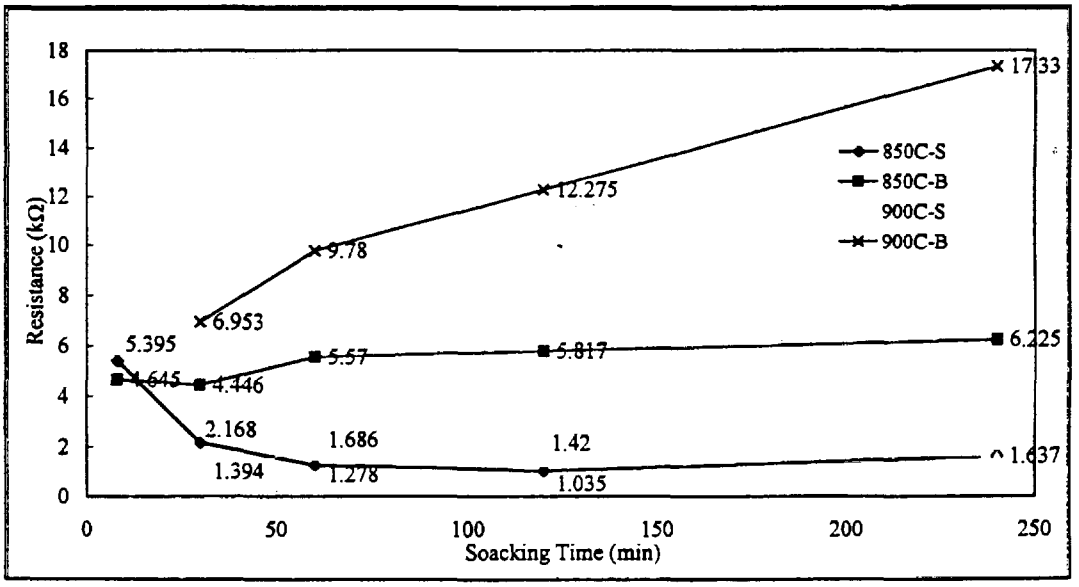
Microstructure of Shoei 1kΩ resistor surface printed on the LTCC substrate.
The sample was fired at 850°C for 30 minutes.



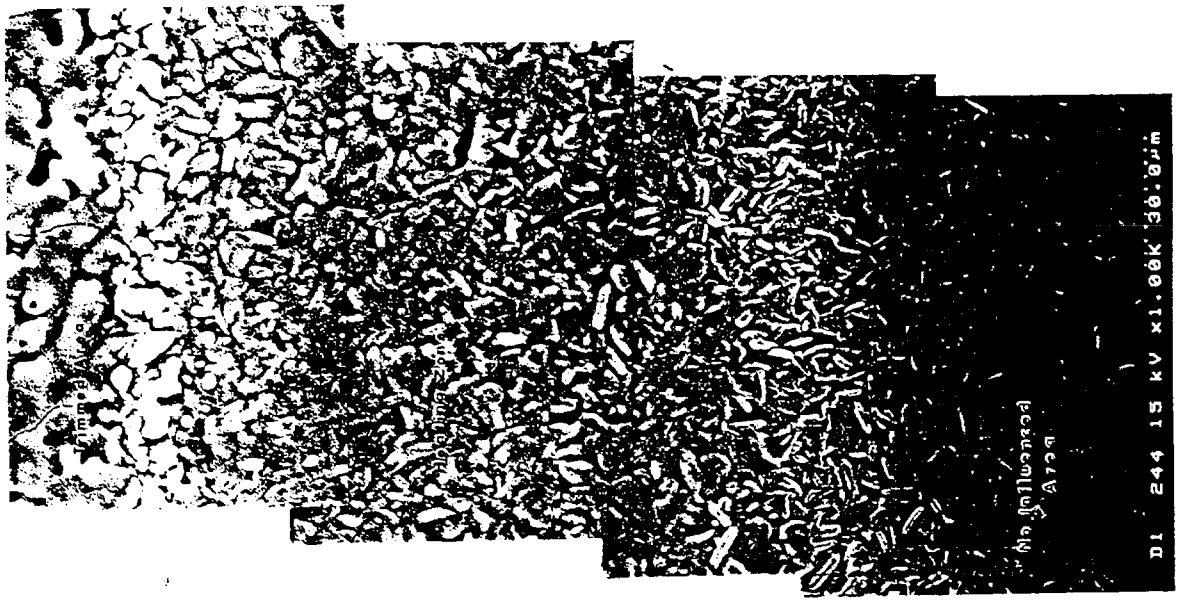
Microstructure of Shoei 1KΩ Resistor Buried in the LTCC Substrate.
The Substrate was Fired at 850°C for 30 Minutes.



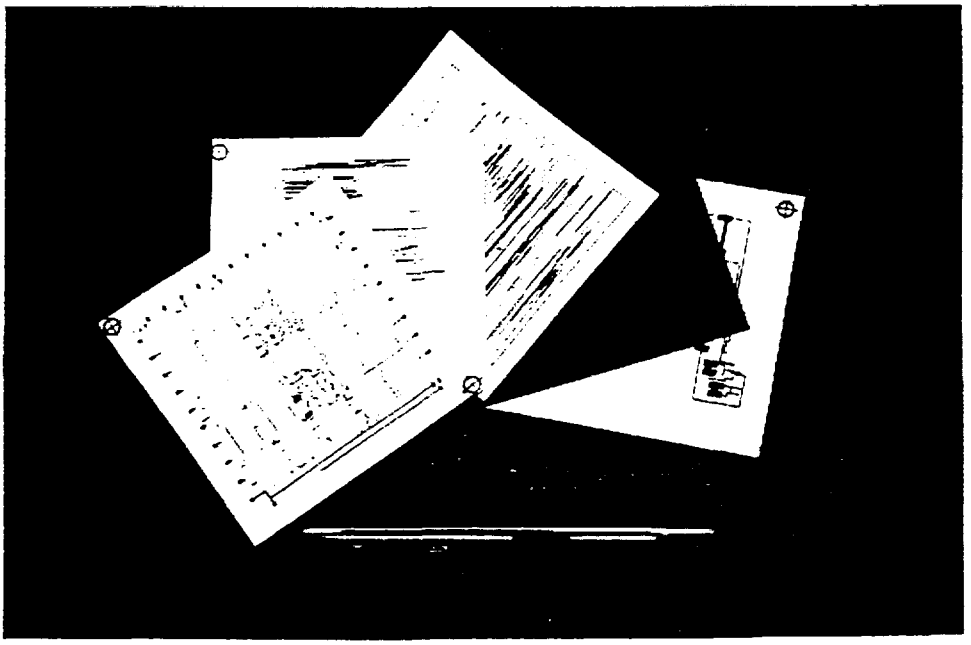
Microstructure of Shoei 1KΩ Resistor Buried in the LTCC Substrate.
The Substrate was Fired at 850°C for 240 Minutes.



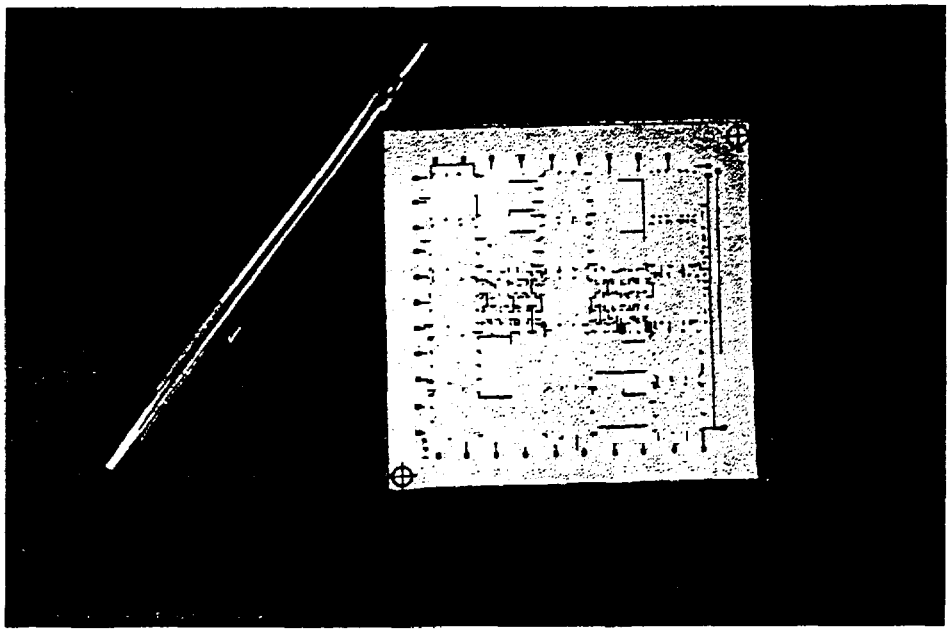
Resistance of Shoei 1kΩ resistor paste printed on and buried in the LTCC substrates. The Length of the resiitors were 10.2 mm.



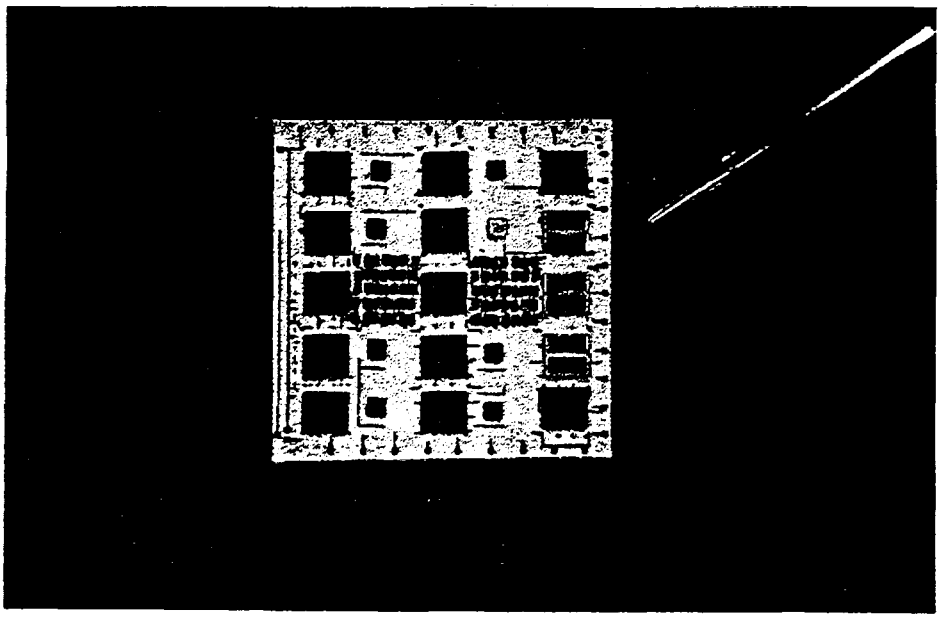
Laser Trimmed of Shoei 10W Resistor Printed on LTCC Substrate



Printed Green Tapes for 14-bit S/D Converter before Laminating



LTCC Substrate for 14-bit S/D Converter



14-bit S/D Converter via LTCC Technique

Summary

1. Low temperature cofirable ceramic substrates with dielectric constant 5.5~6.5 were prepared by cordierite and glass materials.
2. A low temperature sinterable capacitor material with composition $Pb(Fe_{2/3}W_{1/3})_x(Fe_{1/2}Nb_{1/2})_{0.9-x}Ti_{0.1}O_3$ was developed and applied to the LTCC substrates.
3. Commercial resistor materials were printed on and buried in the LTCC substrates.
4. A 14-bit S/D converter prepared via LTCC technique was demonstrated.