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Time Resolved Ion Beam Induced Charge Collection (TRIBICC)

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Abstract

Under this effort, a new method for studying single event upset (SEU) in microelectronics has been developed and demonstrated. Called TRIBICC, for Time Resolved Ion Beam Induced Charge Collection, this technique measures the transient charge-collection waveform from a single heavy-ion strike with a -3db bandwidth of 5 GHz. Bandwidth can be expanded up to 15 GHz (with 5 ps sampling windows) by using an FFT-based off-line waveform re-normalization technique developed at Sandia. The theoretical time resolution of the digitized waveform is 24 ps with data re-normalization and 70 ps without re-normalization. To preserve the high bandwidth from IC to the digitizing oscilloscope, individual test structures are assembled in custom high-frequency fixtures. A leading-edge digitized waveform is stored with the corresponding ion beam position at each point in a two-dimensional raster scan. The

resulting data cube contains a spatial charge distribution map of up to 4096 traces of charge (Q) collected as a function of time. These two dimensional traces of Q(t) can cover a period as short as 5 ns with up to 1024 points per trace. This tool overcomes limitations observed in previous multi-shot techniques due to the displacement damage effects of multiple ion strikes that changed the signal of interest during its measurement. This system is the first demonstration of a single-ion transient measurement capability coupled with spatial mapping of fast transients.

The system has been applied to the study of fast transients in integrated circuits and devices. Single event transients have been measured on CMOS6r n-channel transistors using three heavy-ions: 5-MeV He, 12-MeV C, and 28-MeV Si. These ions have LETs of approximately 0.7, 5, and 15 MeV-cm^2/mg, respectively. The magnitude and shape of single event transients varied with location on test devices. Fast transients were measured from the center of drain regions, while slower transients were measured at the edge of the drain. Measurements were compared to predictions from a 3D transport code that simulates charge transport and collection in semiconductor devices. Differences between measurement and prediction are discussed. Attempts to measure TRIBICC signals in more complex circuits have been limited by noise in the device through control lines and test equipment. Approaches to minimize noise and to further improve the technique are suggested.

Acknowledgments

The authors gratefully acknowledge the contributions to this effort made by John Aurand for calibration and high frequency measurement techniques and Harald Schone, AFRL, for his work as a principal investigator on design and application of the system during the first two years of this effort. Norman Wing contributed significantly to programming the control and data acquisition computers. Peter Winokur, Sandia National Laboratories, is acknowledged for his support and encouragement during this effort.

Contents

Nomenclature

CMOS	Complementary metal oxide semiconductor
DIP	Dual-in-line
FFT	Fast Fourier transform
IBICC	Ion Beam induced charge collection
IC	Integrated circuit
LDRD	Laboratory directed research and development
SEU	Single event upset
TRIBICC	Time resolved ion-beam-induced charge collection

Time Resolved Ion Beam Induced Charge Collection

Introduction

As integrated circuit (IC) feature sizes continue to shrink, ICs are becoming more sensitive to Single-Event Upset (SEU) [1]. In the past, SEU due to naturally occurring energetic heavy ions was only a concern for space-based electronics, but at present levels of integration ICs are becoming sensitive to neutron-induced upsets caused by terrestrial cosmic rays [2]. As a result, SEU is also a reliability concern for avionics and ground based systems. Neutron-induced upset will also be a concern for advanced microelectronics in nuclear weapons systems. As feature size approaches dimensions of 0.1 micron and below as envisioned in the National Technology Roadmap [3], SEU may pose a fundamental limit on the reliability of earth-based microelectronics.

Properly designing ICs to reduce SEU susceptibility while maintaining performance requires an in-depth understanding of SEU mechanisms *and* accurate simulation tools. In previous work, we have pioneered two microbeam testing techniques that give insight into the mechanisms responsible for SEU in ICs. SEU-Imaging identifies the specific transistor structures within a circuit which are sensitive to upset [4]. Alternatively, Ion Beam Induced Charge Collection (IBICC) Imaging produces a quantitative, spatial map of the total charge collection in the circuit [5]. Because the rate at which charge is collected determines upset in static circuits, there is still a need for techniques that measure the transient charge collection processes. Under this labortory directed research and develop (LDRD) program, we have developed a technique called time-resolved ion beam induced charge collection (TRIBICC) that allows measurement of the charge transients resulting from heavy-ion strikes at picosecond time scales as a function of spatial location.

Sandia is currently using three-dimensional transport simulation to study ion-induced charge collection and SEU in silicon devices and circuits. Model based design trade-off studies can easily be one to two orders of magnitude cheaper and months to years quicker than empirical studies, which require expensive and time consuming variations in processing and design. Also, SEU-hardened devices can be made more manufacturable by clearly understanding the trade-offs between SEU sensitivity, performance, and process complexity.

While these simulations provide a great deal of insight into upset mechanisms and trends, there is a dearth of basic experimental data to quantitatively validate simulation results. Detailed spatially and temporally dependent charge collection measurements are needed to experimentally verify transport simulations. However, discrepancies between experimental results and charge collection simulations persist [6-8]. For example, efforts to measure the true shape of charge transients do not reproduce model calculations [6,9,10]. The sampling oscilloscopes used in these earlier experiments required 512 consecutive ion hits at one device position to acquire an entire waveform. Radiation damage induced by repeated ion strikes [11-13] reduces the charge collection by reducing the minority-carrier diffusion length and cannot serve as a definitive standard to which 3D model calculation should be compared. TRIBICC measurements are a key to validating 3-D SEU modeling tools. In addition, although the simulations can compute the SEU threshold, they do not provide information on the cross-sectional sensitive area of an IC. This information, typically obtained from broadbeam experiments at an accelerator facility, is key to predicting upset rates for ICs in the use environment.

The TRIBICC technique developed in this LDRD is ideal for addressing these issues. The best experimental data for model validation is transient charge collection response at well-defined locations of ion incidence. The lack of such data in the past was due to difficulties in measuring picosecond current transients and obtaining precisely located and focused incident ions. Sandia's focused microbeam facility provides just such a source of ions. The addition of a time-resolved capability provides an exact experimental analog to SEU modeling. As developed, the TRIBICC technique scans the ion beam across a region of an IC, providing the desired information on SEU-sensitive cross-sectional area. In this work, simulated charge collection transients of simple devices and test structures were compared to experimental data obtained using the TRIBICC method. The results are a first stop toward validation of the simulation technique.

This report describes the TRIBICC system design and calibration. We present charge collection trasients using simple CMOS transistors and compare these to transients predicted using the DAVINCI™ 3-D transport code. Attempts to apply the technique to the study of SEU in a specialized memory test structure are described. Future applications and improvements to the technique are discussed.

Description of TRIBICC System

Figure 1 shows a block diagram of the TRIBICC setup. The device under test (DUT) is mounted on a high frequency carrier in a vacuum chamber. The ion micro beam is focused to less than 1 μm diameter, with a beam current of not more than 1000 ions/s. A control computer manages and synchronizes the beam exposure to the target and the signal acquisition. Ion induced transients are collected from the test sample and routed to the external RF amplifiers (small signal gain of 220) via a 50 Ω waveguide launcher. Each charge transient with peak amplitude above ~200 mV threshold is captured by the digitizer. When a transient is detected, the ion beam is swept from the target using a high speed (~100ns) beam deflector while the digitizer downloads its data to the control computer. After downloading the 4.5 GHz transient wave digitizer (Tektronix SCD5000) is re-initialized and ready to accept another signal, the beam is redirected to the DUT by turning off the beam deflector. Operating under this condition ensures that a particular measurement location on the device is not damaged by further ion flux during the transient measurement. The entire signal path up to the signal digitizer has a maximum analog bandwidth of at least 18 GHz. This approach ensures that the overall bandwidth limitation, in this case 4.5 GHz, lies with the digitizer and is not further reduced by the quadratic summation of the bandlimited frequency response of all inserted components. Given the 4.5 GHz analog bandwidth limitation of the digitizer, we can expect a system step-response minimum risetime of 77 ps. With a detection limit on the order of 1 mV, the test structure and signal path must have a capacitance of order of 20 pF in order to detect the signal arising from a single heavy ion strike of 20 fC or greater. This limits this technique to small test structures or small test circuits. Photographs of the high frequency test fixture for test transistors are shown in Figure 2.

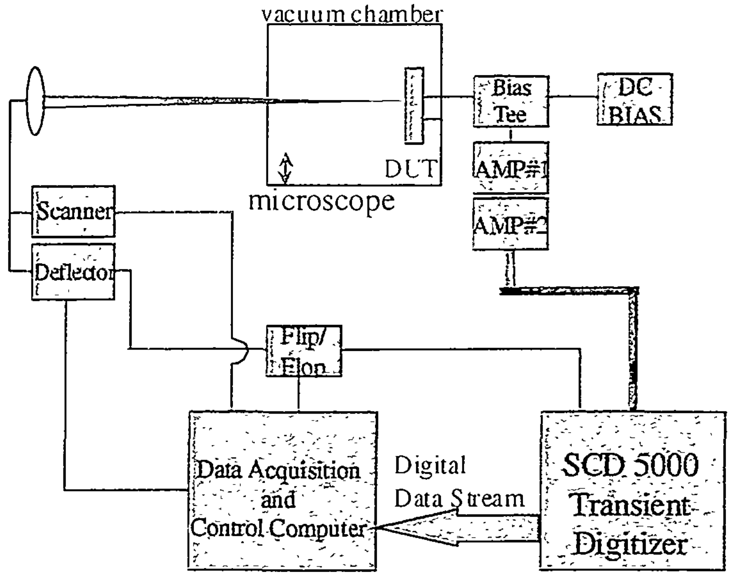


Figure 1 Block diagram of the TRIBICC system.

A. System Calibration

The TRIBICC system exhibits a non-linear gain. A calibration of the system using a pulse generator was used to determine the non-linear factor needed to convert measured pulse amplitudes to actual DUT output response. 2.4 ns wide pulses from a HP8007B pulse generator were directly measured using a 1 GHz TEK680 digital oscilloscope. These same pulses were then input to the TRIBICC amplifiers (Veritek brand amplifiers) and the output was again measured using the TEK680 scope. This 1GHz scope was used in place of the SCD5000 because it is an easier instrument to operate and allows for direct automatic quantification of

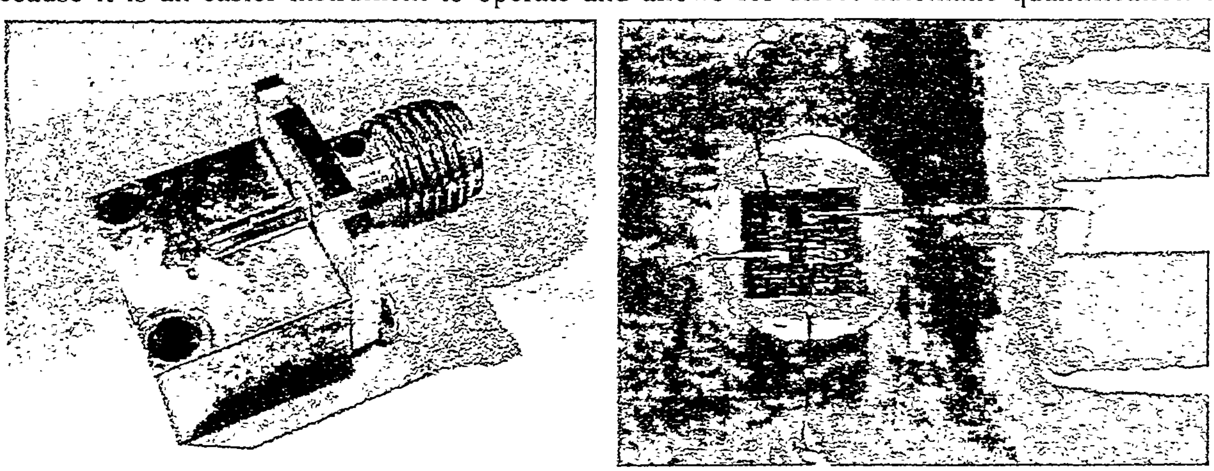


Figure 2: Photographs of the high frequency fixture for measuring TRIBICC signals (left), and a close up of the test transistor to microstrip connection (right).

traces. Comparison of the amplitude measurements of these 2.4ns pulses showed no difference between the responses of the two scopes. Signal cables and connectors were the same as those used in TRIBICC experiments (50Ω cables, 50Ω SMA connectors, all components ≥18 GHz maximum frequency).

Figure 3 shows the results of the measurements. One can see that the amplification is approximately linear below input voltages of 10 mV. Above 10 mV the gain goes nonlinear and quickly reaches saturation somewhere around 20 mV input. This limits the dynamic range of the TRIBICC system somewhat although the ultimate limit of the system is determined by the SCD5000. The SCD5000 requires a signal amplitude of >200 mV to trigger and is limited to a range of ±4V.

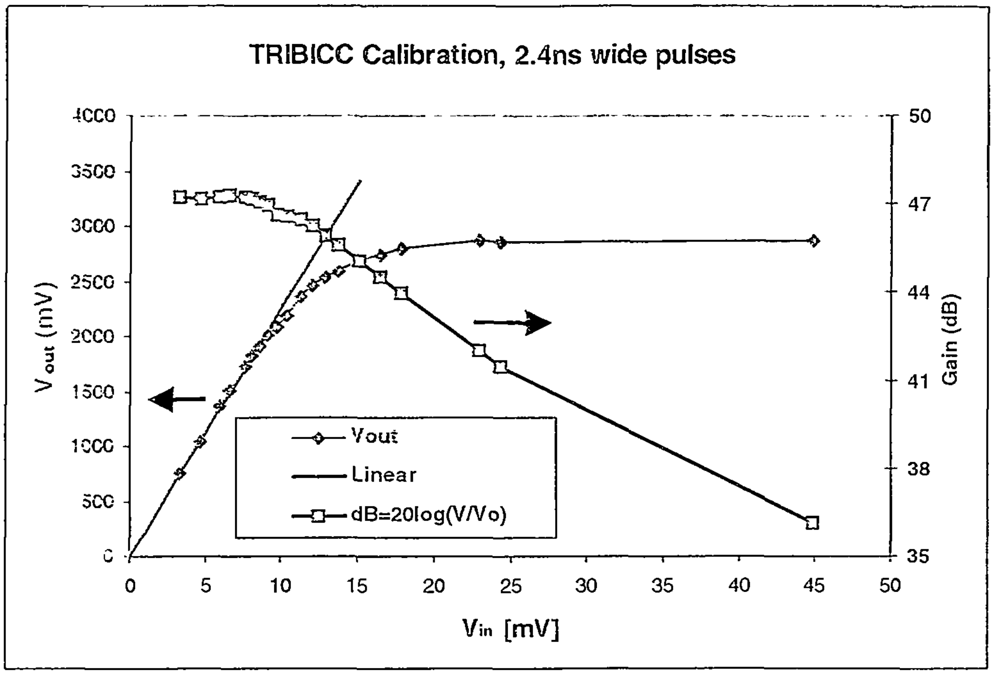


Figure 3. Measured gain of TRIBICC system. Pulses from a HP8007B pulse generator were input to the TRIBICC system and the output pulse measured using a TEK680 1 GHz digital oscilloscope.

The response of the SCD5000 to a fast rising pulse was compared to the response of a 20GHz Tektronix sampling scope. A PSPL 4015C pulser was used to create a –4V step (risetime of ~15ps) pulse with an exponential decay. This pulse was measured both with the SCD5000 and the sampling scope. As expected the limited resolution of the SCD5000 was apparent in the risetime of the step pulse while the peak amplitude was within 10% of that measured with the 20 GHz scope. Figure 4 shows this comparison.

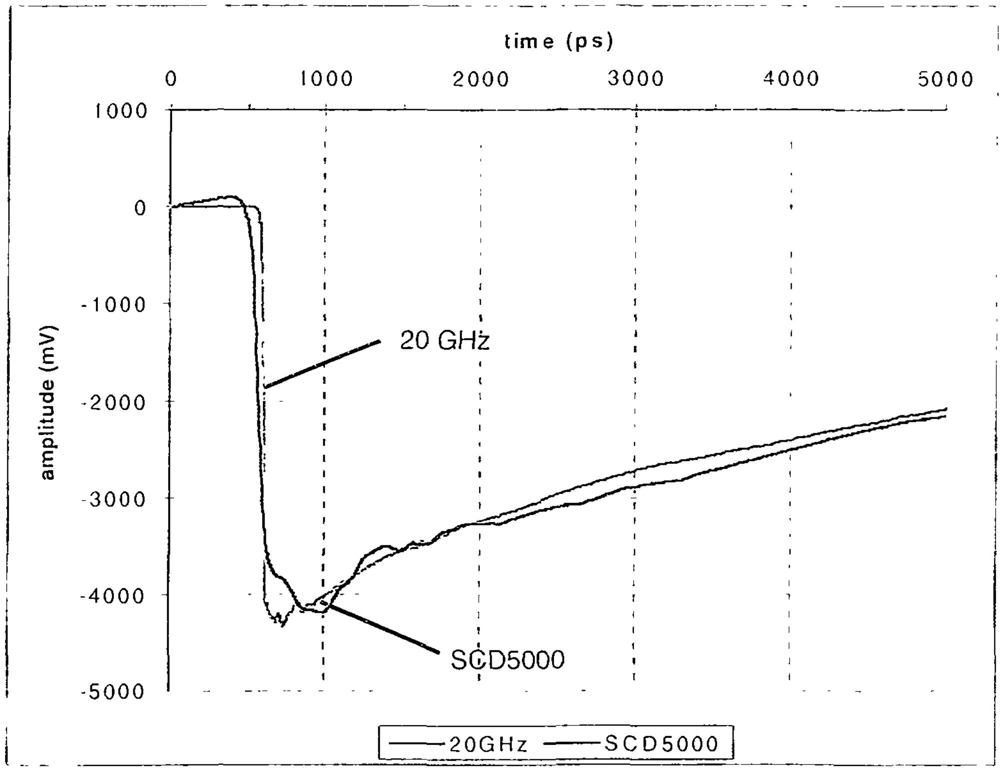


Figure 4. Comparison of SCD5000 4.5 GHz transient digitizer with a 20GHz Tektronix digital sampling scope. Input pulse is a –4V step pulse with exponential decay Step risetime is ~15ps.

Results

A. Transistor Experiments

The TRIBICC technique has been applied to the study of heavy-ion induced transients in simple transistor structures. Devices chosen for this part of the study were n-channel MOS transistors from Sandia's CMOS6r process, and feature a 0.5-μm long channel, with ~3x20 μm sized and 0.25 μm deep drain and source regions. The entire structure is grown on a p-type epitaxial layer 2.7 μm thick, doped at $2x10^{16}/cm^3$. The p-substrate is highly doped at $5x10^{18}/cm^3$. In addition, a p-type halo implant was placed under the source and drain junctions with a peak concentration of $2x10^{17}/cm^3$ at 0.38 μm. The depletion thickness at the drain-halo pn-junction is ~0.15 μm. The devices are capped with standard 2.25 μm thick p-glass.

Figure 5 shows a full set of 4 dimensional data taken during a 30 by 30 μm spatial scan over a single unbiased n-channel CMOS FET drain. The vertical axis represents a 120 ps time slice out of the 5ns acquisition time. One can clearly see the narrow, elongated structure of the drain represented by the dark gray area starting at the 80 ps time slice and continuing to longer times. The amount of current collected at a given point in space and time is represented through the gray scale code. The largest current is collected within the ~3x20μm drain region, while the lower charge is collected from as far as 2 μm from the edge of the drain. These features are consistent with the understanding of near-miss heavy-ion strikes. Dark, narrow lines outside the well-defined drain region are spurious events, unrelated to the device structure and are caused by ion beam scattering of beam defining apertures.

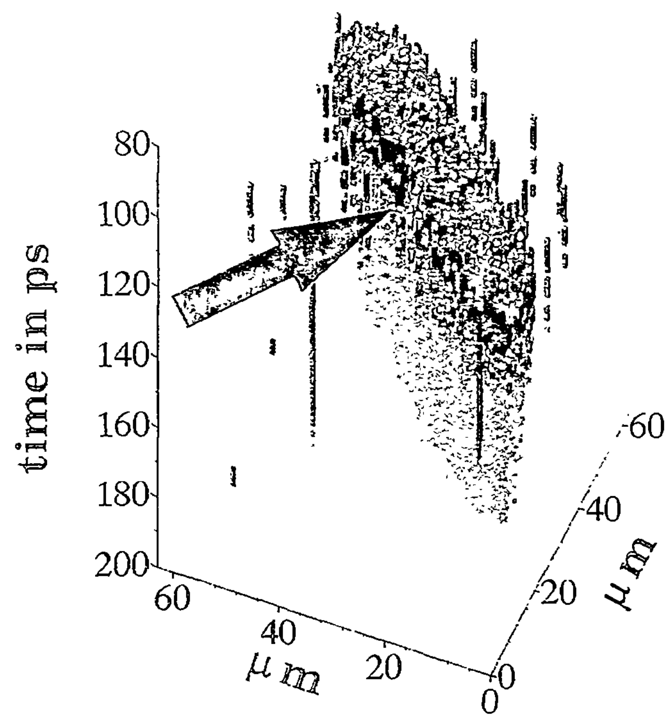


Figure 5. A representation of 4 dimensional charge collection data (2 spatial and one dimension each for time and charge). Arrow indicates the direction and location of line scan data. See text for details. The magnitude of the measured current is represent through the gray scale intensity.

Figure 6 shows an enlarged view of a 2D scan over the same MOSFET. The left-hand side of Figure 6 represents the total charge collected at the drain after a single ion strike. This data map reveals three areas of interest. The dark area in the center of the figure, and two lighter shaded areas to the left and right. These areas have been optically identified as the drain area in the center, the gate area to the right and the 1-2 μm area directly adjacent to the drain. Most of the charge (on average 350 fC) is collected in the center of the drain. Ions striking within 1 to 2 μm of the drain diffusion area or close to the gate produce charge transients with an average collected charge of 260 fC.

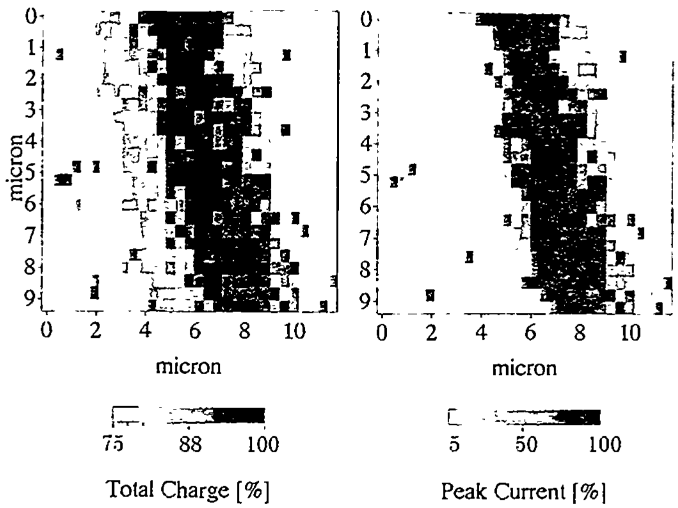


Figure 6. 2D scan over part of MOSFET. Left hand map depicts total charge collected at drain and right hand map shows peak currents collected at drain.

The total charge alone is not a definitive measure for the SEU-sensitive region. The peak current collected at a node can determine, for example, if a static RAM cell will change its logic state. The subsequent total charge collected, albeit slow, will then determine if the device remains in the new (incorrect) logic state [14]. The right hand side of Figure 6 depicts the peak current transients measured. The same three distinct areas of interest are discernible. The area to the left of the drain shows peak currents of only 5 to 10% of the maximum center drain currents The dark central area coincides with the extent of the drain. The lower peak current region may be less likely to produce upsets, although the total collected charge is only slightly less than in the drain. Ions striking the near-gate areas show peak currents as high as 30% of the center drain strikes.

The maps in Figure 6 do not reveal the temporal evolution of the collected charge. Instead, a linear horizontal cut perpendicular to the extent of the drain, indicated by the bold arrow in Figure 5, is shown in Figure 7. For each new trace, the ion beam was advanced on average by 350 nm (±250 nm). Ion hits too far from the drain to produce a measurable transient were omitted. The time axis represents a 3.5 ns time slice. A cross sectional view of the transistor and scan direction of the ion beam is inserted into the lower right hand corner of Figure 7. This figure shows three distinctly different groups of current traces.

The group of five traces labeled "drain edge" originates from ion strikes hitting up to 2 μm from the edge of the drain. This group of current transients has a rise time of ~750 ps and a decay time of about 100 ns. On average, 270 fC are collected at the drain. The pulse shape of these traces is consistent with a purely diffusion dominated charge collection. While the pulse shape does not vary significantly with strike position the amount of total charge collection is reduced as the ions strike farther from the drain edge.

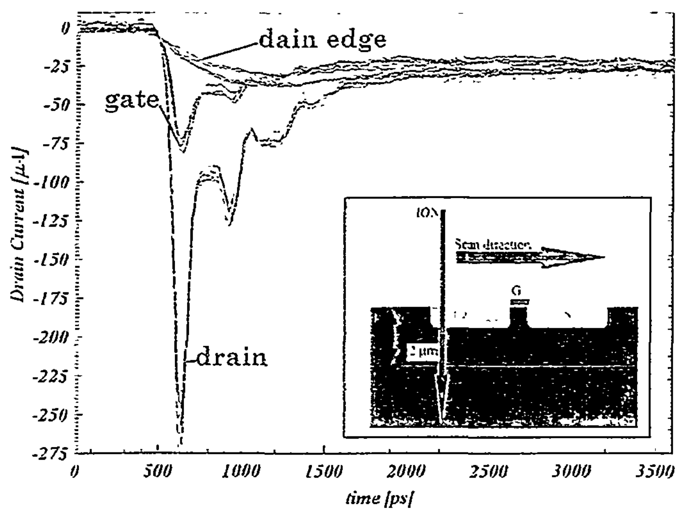


Figure 7. Current traces induced by ions striking near the drain edge, within the drain region and through the gate. Dotted trace represents a slit scattering event.

In contrast, ions traversing the drain region induce large (about -275 μA) signals. This group of 8 traces is labeled "drain" in Figure 7 and exhibit a bandwidth limited 70-75 ps rise time and 100 ps FWHM wide peak with a tail of about 10 ns decay time. The fast peak is evidence of drift charge collection within the depleted pn-region formed by the drain to substrate region. Also, we expect the formation of a funnel into the epitaxial layer that will contribute to the fast charge collection. The slowly decaying component is consistent with diffusive charge collection from below the drain's n^+-region. The apparent ringing has a delay time of ~350 ps and is believed to originate from the gate, source and bulk connections to ground, which in this case are through 1 mil Au bond wires. The rise time of the fast drain center signals are only limited by the experimental bandwidth, indicating that the drift/funnel signal is appreciably faster than the experimental resolution.

The total measured charge collected in the center of the drain is on average 350 fC, of which less than 80 fC is collected by the prompt drift/funnel charge collection process. Approximately 270 fC of this drain signal is due to diffusive charge collection.

The last group of 3 traces, labeled "gate", arises from ion strikes traversing very close, or in fact through, the gate region. These transients show the same but smaller drift assisted charge collection peak with a diffusion component that is about 10% smaller than the diffusion components from drain or near-drain ion strikes. The entire charge collected for these strike locations is on average 270 fC. The fast current peak arises from gate strikes or drift collection from a perturbation in the nearby drain depletion region (funneling from a near miss). The fast charge collection component of this transient may be an indication of very fast diffusive transport or may arise through the deformation of the lateral drain depletion region into a funnel like field extension that reaches under the gate. The slightly lower diffusion component is probably due to the proximity of the grounded source since a fraction of the excess charge is likely to be collected by the source.

It is noteworthy, that aside from spurious slit scattering events, all current traces are tightly grouped. This indicates a very repeatable and stable measurement system.

B. Radiation Damage

To answer the question of how radiation damage will effect the charge collection process, we have measured the transient signals from three regions of a test transistor as a function of ion flux to the region. Figure 8 shows the damage effects of 8, 204 and 540 ions/μm^2 on drift and diffusive charge collection. The ion beam was stepped over the transistor with a step size of only 125 nm. Each of Figs. 8a through 8c show the charge collection efficiency as dose accumulates in a specific region of the device. In the near drain region (Fig. 8a), one can discern prompt charge collection aided by a lateral funnel that is presumably reduced progressively through the accumulation of radiation induced scatter sites. For strikes directly to the drain region (Fig. 8b), drift charge collection within drain strikes is not affected, while the diffusive charge collection is strongly reduced after 204 ions/μm^2. With the assumption that all prompt charge collection in the gate region is aided through the development of a lateral funnel, the reduction of drift and diffusive charge collection observed in Fig. 8c can tentatively be explained by an increase in scattering sites.

C. Comparison to 3D Simulations

This series of experiments presented was geared not only to further the understanding of the charge collection process, but also to validate numerical simulations of the charge collection process. 12-MeV carbon ion hits to single transistors were simulated with the three-dimensional DAVINCI™ code [15] using Sandia CMOS6r process information as input.

The current transient results of the DAVINCI™ calculations implicitly assume an infinite analog bandwidth from the device drain to the current measuring point. The measurement setup used in this experiment, however, has a -3db analog bandwidth of 5 GHz. Consequently, any current transient from the device with a bandwidth higher than the experimental resolution will be broadened. Note that the total charge collected will not change, but the current transient will have a different temporal evolution.

To achieve a meaningful comparison between the calculations and experiments, the simulated current

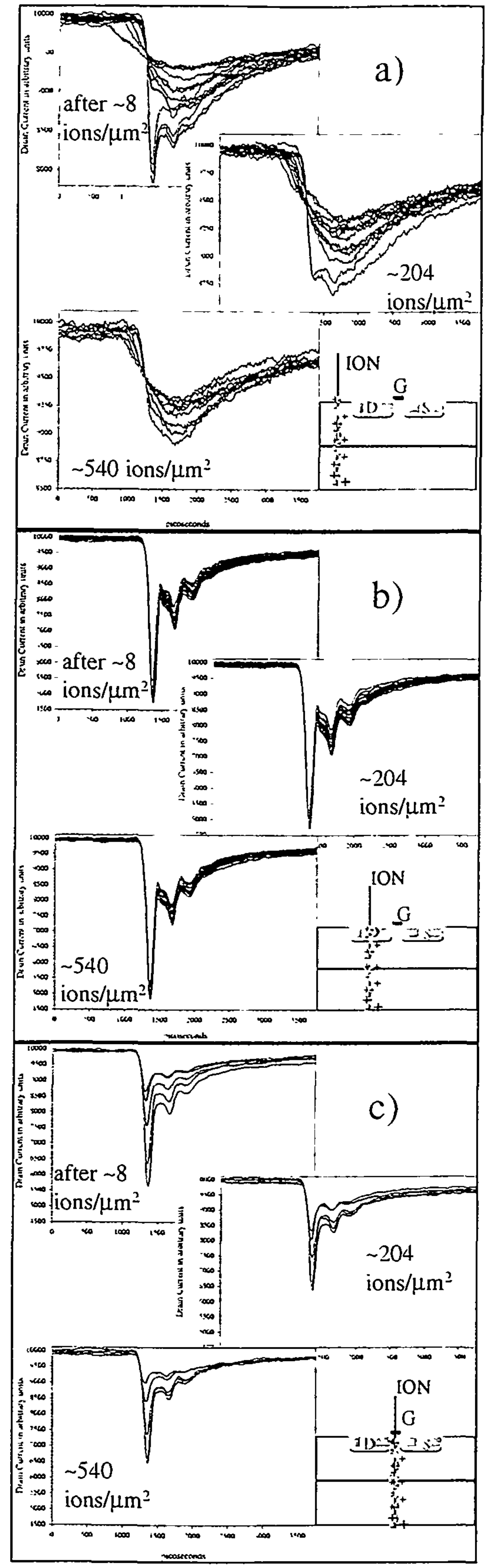


Figure 8. Effect of radiation damage on charge collection mechanisms for a) near drain region, b) drain region, c) gate region.

transients were folded with the experimental bandwidth as follows:

$$f(t) = \int_{-\inf}^{+\inf} f_m(t) \times g(t)dt \tag{1}$$

where f_m is the calculated current transient, and g(t) is a Gaussian distribution given by

$$g(t) = \frac{1}{\sqrt{2\pi}} \exp\left[\frac{-(t-t_0)^2}{2\sigma^2}\right] \tag{2}$$

Here, t_0 = 75 ps and σ is the distance from the centroid (t_0) to the inflection points (~FWHM) of the gaussian function. A value of σ=4×10^{-11} was chosen, to result in a risetime of 70 ps for the transformed current transient.

Figure 9 compares the experimental curves of ion strikes to the same regions as shown in Figure 7 with corresponding DAVINCI™ calculations. The calculation results have been scaled to the measurement for easier comparison. The calculations reproduce the experimental data very well. In particular, the distinct rise-time and peak height differences between drift vs. diffusion are well reproduced. The ratio of drift to diffusion charge collection at late times, however, is not accurately reproduced in the DAVINCI™ simulations. For off-drain ion strikes, the diffusive charge collection is underestimated by about 50%. This difference can arise in part through an incorrect estimate of the diffusion length and life time of injected minority carriers. Furthermore, small variations in the ion strike distance to the drain area will result in significant changes in the amount of diffusive charge collection. Hence, the experimental uncertainty of the ion strike location of about 0.5μm may significantly contribute to the observed discrepancy.

For ions striking the drain center we observe that the calculated drift charge collection is overestimated by less than 15%. Yet, the magnitude of diffusion is underestimated by a factor of 2-3. This difference cannot be accounted for through the uncertainty in strike location as the shape of the transient clearly indicates a center drain strike. Nor is it possible to explain the difference through inaccurate minority carrier lifetime estimates. Current transients induced by ion strikes in the gate region are also well reproduced by the DAVINCI™ calculations. Note that the DAVINCI simulations exactly predict the measured ratio of peak drift current magnitude between drain-center and gate-center strikes.

The total charge deposited by a single 12 MeV Carbon ion within the 2.7 μm thick epitaxial layer, calculated using TRIM [16], is ~140 fC. The charge deposited in the substrate material below the epi layer during the remaining ion path of 5.6 μm is ~270 fC. We conclude from the experimental results that charge is collected from well below the epitaxial layer in order to account for the measured charge in excess of 140 fC. The peak height of the prompt (~100ps) charge collection seen in the drain region is a clear indication that funneling occurs, because too much charge is collected to have come from the original depletion region alone.

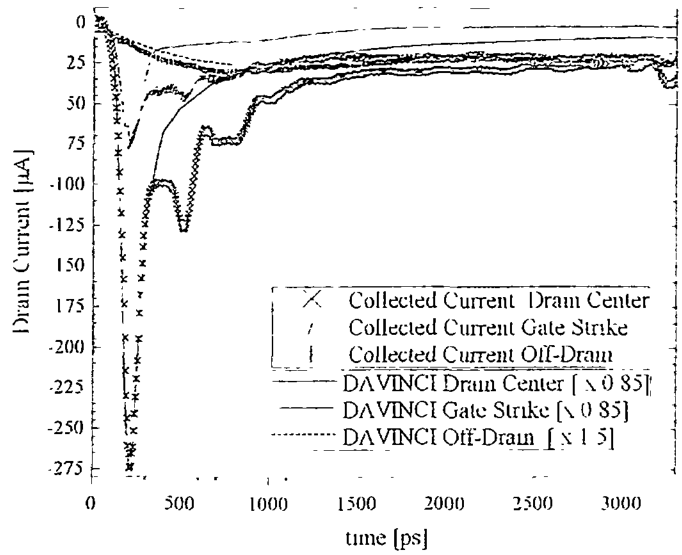


Figure 9. Measured current transient for a single 12 MeV Carbon ion striking the drain center and 1-2 µm off-drain, respectively DAVINCI™ calculations are scaled to permit easy comparison to the data.

The experiment permits the first reliable estimate of the funneling depth. We have calculated an average energy deposition for 12-MeV carbon ions in the epitaxial layer of 120 eV/Å. By subtracting from the measured center drain hit current the diffusive charge collection component and the charge collected in the 0.15µm thick depletion region under the drain, one can get a funneling depth of ~1.5µm. Subtracting the diffusive charge collection from the drift charge collection adds an uncertainty of 10% to the funneling depth estimate because we are unable to estimate the amount of diffusive charge collection during the formation of the funnel. It is expected that an increased drain bias will strongly enhance the prompt charge collection to the point of a funneling depth comparable to the epitaxial layer thickness.

In general, the 3D DAVINCI™ calculations reproduced the measured transient very well. In particular, we have shown that the drift charge collection agrees within the experimental error of the measurements. However, the diffusive charge collection, especially for center drain strikes, is underestimated. Future work is planned to expand the experimental efforts to include other ions species, different FET bias states and to achieve a higher charge collection bandwidth.

D. Application To SEU in ICs

While test transistors are useful structures for measuring current transients in pn junctions, single event upset occurs in only higher level circuits such as memories and latches where a current transient results in a change of state. A special low-capacitance test circuit was designed and fabricated with the intent of directly measuring the current transients during upset. Because only one ion with sufficient LET is required for to upset a memory circuit, oxide charging and nuclear displacement damage to the stuck FET is not an issue and cannot influence the resulting transient measurement. A schematic of the test circuit is shown in Figure 10. Two memory bits (cell 1 and cell 2) are connected through control circuitry to a bi-directional I/O buffer. The R/W

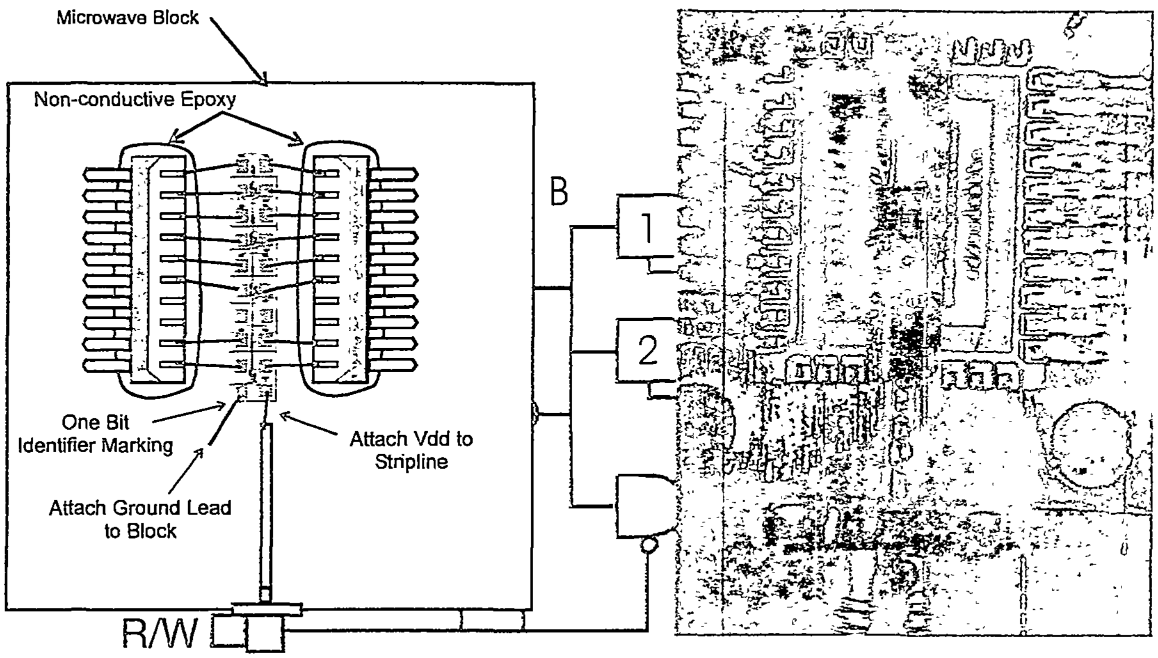
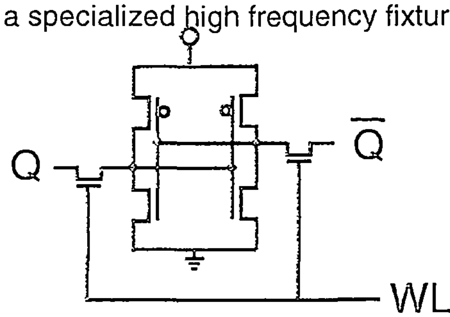


Figure 11: Diagram and photograph of memory test chip mounted on a specialized high frequency fixture.



b)

Figure 10: Schematic of 1) memory test circuit with control logic, and b) single memory cell.

input controls whether information on the I/O is read from or written to a memory cell that is selected through word lines (WL1 or WL2). Four duplicates of this circuit were implemented on a single test chip with different memory cell transistor widths (W=min or W= 2x min) and with and without feedback resistance in the memory cell cross-coupling.

Completed test chips were mounted onto a specialized fixture, shown in Figure 11. Connection to control lines was accomplished through a ceramic dual-in-line (DIP) package that was sawn in half, and half subsequently epoxied to the microwave block. Wire bonds attached control line bond pads on chip with DIP wire pads, and external connection was made to the DIP leads. The chip power supply bond pad was connected via microstrip line to a high frequency SMA connector mounted on the side on the microwave block. Power was provided and charge collection transients were measured through this connection.

We were able to measure IBICC and SEU images on the memory test chip using previously developed techniques. However, we were not able to measure TRIBICC signals from this test structure due to excess noise on the V_{DD} line. The source of the problem was antenna noise on the control line connections. An optical interface circuit to the control lines was designed but wasn't implemented before the completion of activity under this LDRD.

2D Charge Collection Maps

In the future, extensive computer simulations of a full TRIBICC experiment will be performed to produce a 2D map of charge collection and an estimation of the upset cross-section. While extremely computationally intensive, this will serve as an additional sanity check on the code validity and will provide vital information for correlating simulation results to TRIBICC cross-sectional maps. Using this information and TRIBICC data, a technique will be developed for reducing the computational load in estimating the upset cross-section from simulation results. Broad-beam experiments will be used to verify predicted cross-sections. Design trade-space analysis will be performed using simulations to demonstrate the simulation-based methodology for designing radiation-hardened devices. The aim of the experiments is to eventually enable a comprehensive comparison between transport calculations and the time-dependent charge migration after an ion strike in a fully functional IC. These complex calculations require a massively parallel 3D modeling code. A massively parallel version of DAVINCI™ is being developed under a separate effort, but at the time of this writing was unavailable for comparison of experimental and predicted measurements.

Future Improvements

The experimental setup described in this paper is well suited to allow a bandwidth improvement to 15 GHz without any further modifications. Previous work has demonstrated a factor of 4.5 bandwidth improvement for a similar system through a data compensation algorithm that exploits the slowly rolling off amplitude response of the digitizer [17]. In particular, the higher bandwidth capabilities will result in a more rigorous comparison to model calculations. Sensitivity of the system could be improved with better (higher bandwidth, higher gain) amplifiers and better methods of signal transfer from the DUT. The latter may not be feasible as it may require special direct processing on the device itself, so at best could only be utilized in specially designed test structures. Implementation of full 3D ion induced charge collection codes such as DAVINCI™ on massively parallel frameworks is necessary in order to compare simulated an experimental charge collection maps.

Summary

The TRIBICC configuration allows measurement of current transients on a device under test (DUT) to a maximum analog bandwidth of at least 20 GHz. At present, overall system response is limited by the 5 GHz digitizer and is not further reduced by other system components. Each charge transient with peak amplitude above ~1 mV threshold is captured by the system and a high speed (~100ns) beam deflector rapidly sweeps the beam off the DUT to minimize further heavy ion damage.

We have measured spatially-dependent current transients after single strikes on 0.5 µm n-channel transistors manufactured at Sandia National Laboratories using 5-MeV He, 12-MeV C, and 28-MeV Si ions. Two-dimensional scans resulted in up to 1024 spatial charge collection maps, each representing a time slice as short as 5 ps of the charge collected. These single-ion transient measurements, as well as the spatial mapping of fast transients, have never before been achieved.

Measurements using 12-MeV carbon ions clearly show the dependence of current transients on spatial location. Strikes hitting up to 2 µm from the edge of the drain have a rise time of ~750 ps and a decay time of about 100 ns, consistent with a purely diffusion dominated charge collection. In contrast, ions traversing the drain region induce large (about -275 µA) signals and exhibit a bandwidth limited 70-75 ps rise time and 100 ps FWHM wide peak with a tail of about 10 ns decay time. The fast peak is evidence of drift charge collection within the pn-junction depletion region and the funnel region that extends below the original junction, while the slowly decaying component in this transient is consistent with diffusive charge collection from below the drain's n+-region. Some ringing is evident in the measurements and has a delay time of ~350 ps and probably originates from the gate, source and bulk connections to ground. The rise time of the fast drain center signals are only limited by the experimental bandwidth, indicating that the drift/funnel signal is appreciably faster than the experimental resolution.

Measured current transients have been compared to the corresponding simulations using the DAVINCI™ 3D code. In general, the calculations reproduce the experimental data. The distinct rise-time and peak height differences between drift v s. diffusion are well reproduced. The ratio of drift to diffusion charge collection at late times, however, is not accurately reproduced. For off-drain ion strikes, the diffusive charge collection is underestimated by about 50%. This difference can arise in part through an incorrect estimate of the diffusion length and lifetime of injected minority carriers. Furthermore, small variations in the ion strike distance to the drain area will result in significant changes in the amount of diffusive charge collection.

The TRIBICC technique was also applied to the study of single event upset mechanisms in memory devices. Single event transients may provide useful insights into the dynamics of upset and have never been directly measured. A specialized memory test structure was mounted on a high frequency fixture and transient signals in the power supply line were measured to detect current transients resulting from upset in the memory cells. This measurement was limited by noise that was picked up in control lines into the device. A modified test configuration using opto-coupler isolation to reduce noise has been designed but not implemented at this time.

A goal to perform a detailed comparison between TRIBICC measurements and 3D simulations over a full memory cell was not completed, because the essential massively parallel version of DAVINCI™ was not completed in FY99. A source code license was purchased (with non-LDRD funds) and a memory scaleable version of DAVINCI™ has been developed (with

ASCI funding) that runs on one node of the Janus machine. A fully parallelized version scaleable to the order of 100 processors will be completed in FY00.

References

1. E. L. Petersen and P. W. Marshall, "Single Event Phenomena in the Space and SDI Arenas," *J. Rad. Effects: Res. Eng.*, vol 6, no 2, p. 1 (1988).
2. A. Taber and E. Normand, "Single Event Upset in Avionics," *IEEE Trans. Nucl. Sci.*, vol. 40, pp. 120-126, 1993.
3. "The National Technology Roadmap for Semiconductors: Technology Needs," Semiconductor Industry Association, p. 46, 1997.
4. K. M. Horn, B. L. Doyle, D. S. Walsh, F. W. Sexton, and G. L. Hash, "Application of the Nuclear Microprobe to the Imaging of Single Event Upset," *Scanning Microscopy* 5, p. 969, 1991.
5. F. W. Sexton, K.M. Horn, B.L. Doyle, J.S. Laird, M. Cholewa, A. Saint, and G.J.F. Legge, "Ion-beam-induced charge-collection imaging of CMOS ICs," *Nucl. Instr. and Meth. In Physics Research B*, vol. 79, p. 436-442, 1993.
6. A.R. Knudson and A.B. Campbell, "Comparison of Experimental Charge Collection Waveforms with PISCES Calculations," *IEEE Trans. Nucl. Sci.*, vol. 38 (6), pp. 1540-1545, 1991.
7. H. Dussault, J.W. Howard, Jr., R.C. Block, M.R. Pinto,W.J. Stapor, and A.R. Knudson, "High Energy Heavy-Ion-Induced Single Event Transients in Epitaxial Structures," *IEEE Trans. Nucl. Sci.*, vol. 41 (6), pp. 2018-2025, 1994.
8. K.M. Horn, P.E. Dodd, M.B.H. Breese, and B.L. Doyle, "Verification of three-dimensional charge transport simulations using ion microbeams," *Nucl. Instr. Meth. In Physics Research B*, vol. 130, pp. 470-477, 1997.
9. R.S. Wagner, J.M. Bradley, N. Bordes, C.J, Maggiore, D.N. Sinha, and R.B. Hammond "Transient Measurements of Ultrafast Charge Collection in Semiconductor Diodes," *IEEE Trans. Nucl. Sci.*, vol. 34 (6), pp. 1240-1245, 1987.
10. Nashiyama, T. Hirao, T. Kamiya, H. Yutoh, T. Nishijima, and H. Sekiguti, "Single-Event Current Transients Induced by High-Energy Ion Microbeams," *IEEE Trans. Nucl. Sci.*, vol. 40 (6), pp. 1935-1940, 1993.
11. T. Hirao, I. Nashiyama, T. Kamiya, and T. Nishijima "Effects Of Micro-Beam Induced Damage on Single-Event Current Measurements," *Nucl. Instr. Meth. In Physics Research B*, vol. 104 (1), pp. 508-514, 1995.
12. M.B.H. Breese, "A Theory of Ion Beam Induced Charge Collection," *J. Appl. Phys.*, vol. 74 (6), pp. 3789-3799, 1993.

13. F.W. Sexton, K.M. Horn, B.L. Doyle, M.R. Shaneyfelt, and T.L. Meisenheimer, "Effects of Ion Damage on IBICC and SEU Imaging," *IEEE Trans. Nucl. Sci.*, vol. 42 (6), pp. 1940-1947, 1995.

14. P.E. Dodd and F.W. Sexton, "Critical Charge Concepts for CMOS SRAMs," *IEEE Trans. Nucl. Sci.*, vol. 42 (6), pp. 1764-1771, 1995.

15. DAVINCI 4.0 User's Manual (Technology Modeling Associates, Inc., 1997).

16. J. F. Ziegler, J. P. Biersack and U. Littmark, The Stopping and Range of Ions in Solids, New York: Pergamon Press, 1985.

17. P. E. Patterson, J.F. Aurand, C. A. Frost, "15-GHz Bandwidth Enhancement of Transient Digitizers in a Portable Data Acquisition System," Sandia Report, SAND93-2280.

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