Laboratoire de l'Accélérateur Linéaire

NEMO-3 Calorimeter Electronics

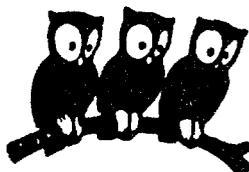## P. Bernaudin, C. Cheikali, B. Lavigne

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Abstract

The calorimeter electronics of the NEMO-3 double beta decay experiment fulfills three functions:

- energy measurement of the electrons by measuring the charge of the pulses,
- time measurement,
- fast first level triggering.

The electronics of the 1940 Scintillator-PM modules is implemented as 40 "9U x 400mm VME" boards of up to 51 channels. For each channel the analog signals conditioning is implemented as one SMD daughter board. Each board performs 12 bit charge measurements with 0.35 pC charge resolution, 12 bit time measurements with 50 ps time resolution and a fast analog multiplicity level for triggering.

The total handling and conversion time for all the channels is less than 100 μs.

The electronics will be presented as well as the test system.

I. INTRODUCTION

The calorimeter of the Neutrinoless Experiment with MOlybdenum (NEMO) is intended to provide measurements of energy from 20 KeV to 12 MeV and time of flight up to 5 ns of the electrons from the double-beta decay process, particularly without neutrino emission [1].

The electron detection is performed by 1940 plastic scintillator-photomultiplier modules covering the 2 concentric cylindrical walls and the top and bottom end caps.

The counting rates in running conditions are estimated at a few tens of Hz per photomultiplier, and can reach a few tens of kHz for calibration with radioactive sources. In order to do fast acquisition in calibration conditions, conversion times must not exceed 100 μs.

The level 1 trigger is taken from the calorimeter and typically requires a coincidence between 2 Scintillator-PM modules. The results of the tracking device are associated with level 1 to make the level 2 trigger.

II. SYSTEM DESCRIPTION

A diagram of the system is shown in figure 1. The front-end electronics board has been designed to handle one half sector of the NEMO experiment apparatus. The 40 boards sit in 3 VMEbus crates, type V430, as specified by CERN [2].

The control and readout of the crates are performed via the inter-crate VICbus by a CES RIO 8062 computer module

equipped with a PowerPC 604E-300MHz CPU chip. The CASCADE [3] under Lynx-OS software system has been implemented and can achieve the acquisition requirements of a few hundred Hz in running conditions and a few thousand Hz for calibration with radioactive sources.
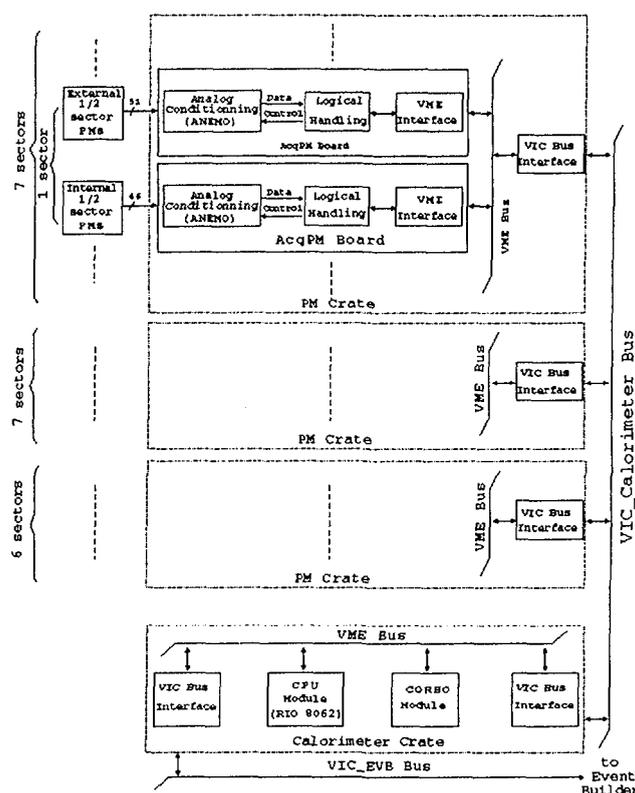

Figure 1. Calorimeter System Electronics.

III. PHOTOMULTIPLIERS ELECTRONICS

The choice of low radioactive materials is essential for the photomultiplier tubes and their high voltage distributions. For this purpose the bases are made of phenolic paper printed circuit (FR2) equipped with polycarbonate or polypropylene capacitors.

The high voltages are set from 1.1 kV to 1.5 kV for the 5" PMs and from 1.5 kV to 1.9 kV for the 3" PMs with the base current being less than 250 μA. One high voltage channel supplies three close gain PMs. The addition of one appropriate resistor achieves the individual gain adjustment.

IV. ANEMO BOARD (Daughter)

The Analog-NEMO daughter board, shown in figure 2, delivers three signals:

- Q OUT: proportional to the charge (gate = 70ns),
- T OUT: proportional to the time between the low threshold crossing and a signal (STOP) coming from the trigger,
- DISCRI OUT: logic signal coming from the high threshold crossing for the trigger.
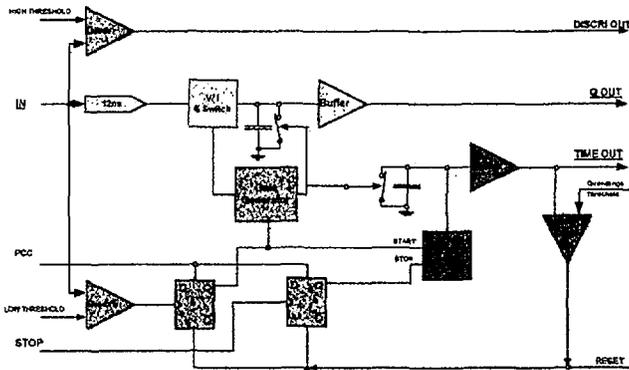

Figure 2. ANEMO Board Block-Diagram.

Two discriminators are used:

- the low threshold one starts the charge integration and time measurement,
- the high threshold one, modified to work as a one shot, delivers a signal to the analog multiplicity electronics.

The time walk due to the leading edge discriminator is corrected off line, using the charge information and the input rise time knowledge.
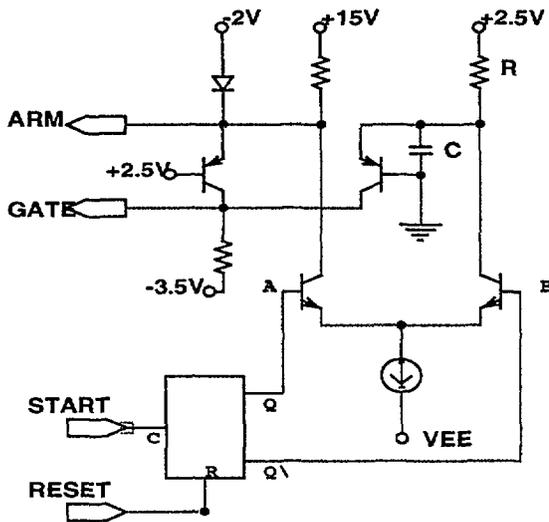

Figure 3. ANEMO Gate Generator.

The gate generator, shown in figure 3, is made with 4 transistors. It gives 2 translated outputs:

- one (GATE) for the charge integrating command : R and C set duration.

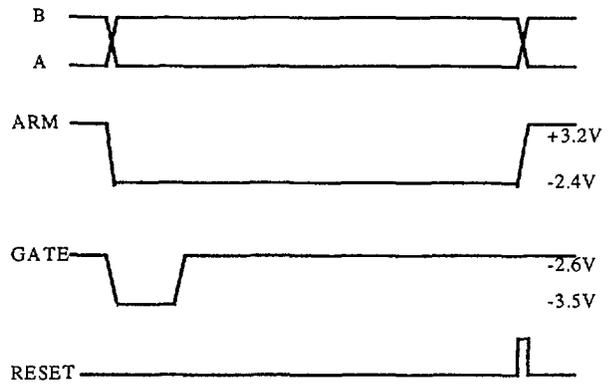- one (ARM) to open the two MOS transistors in parallel with the integrating capacitors.

Figure 4. Gate Generator Timing.

The charge integrating circuit is a standard one. It is AC coupled.

The Time Amplitude Converter (TAC) circuit, shown in figure 5, uses 3 transistors. The current injected at the emitters connection is switched from Q1 to Q2 on START and from Q2 to Q3 on STOP. The Q2 collector current charges "C" between START and STOP. After STOP, the Q3 collector current is used to deliver a Valid channel signal (VAL CHAN).
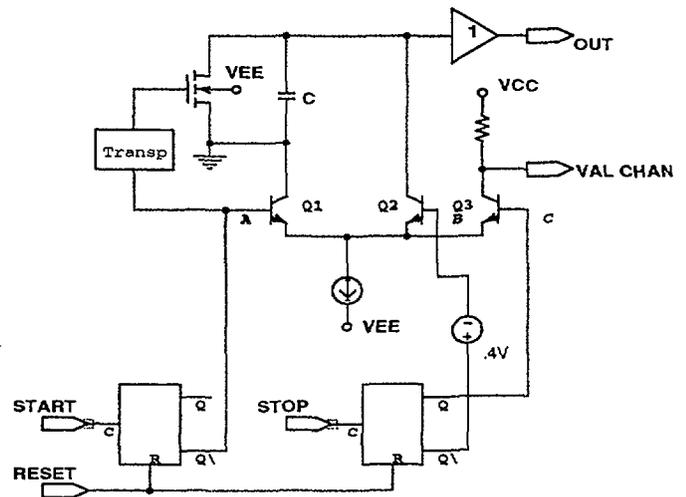

Figure 5. ANEMO Time Amplitude Converter.

An over range detection is used to reset the logic if there is no STOP.

Due to the small number of circuits to be made, it was decided not to design an ASIC but to use SMD standard components. We succeeded in a short design time and a competitive price. The daughter board area is 23x40 mm^2 and the price is 31 Euros for a fully assembled and tested circuit.

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V. CALORIMETER BOARD (Mother)

The calorimeter board shown in figure 6, houses up to 51 ANEMO daughter boards to process the photomultiplier signals of 1/2 NEMO sector. This distribution requires a large critical 10 layer printed circuit board. A unique ground plane is used as a voltage reference and as a shield between contiguous boards in a crate.
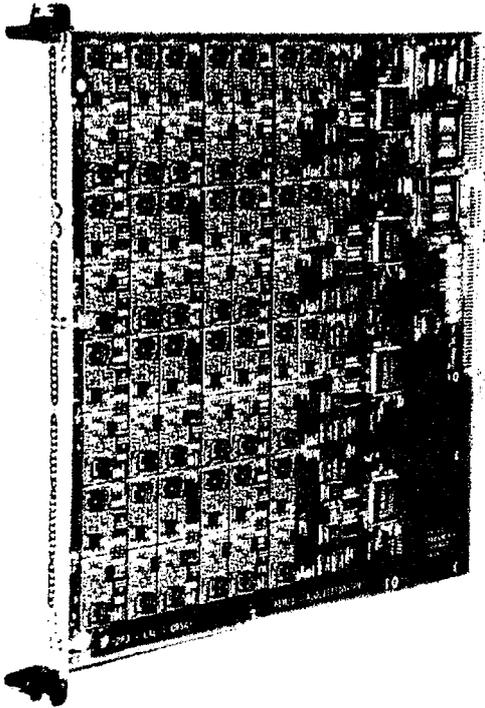

Figure 6. Calorimeter Board.

To fulfill the resolution and the timing specifications, the 51 channels of one board are distributed among 4 groups as shown in figure 7. Each group concurrently performs identical functions:

- the low level threshold supplies: one 8-bit DAC per channel , lsb = 1 mV,
- the high level threshold supplies: two 8-bit DAC per group, lsb = 4 mV,
- the hit channels identification and address coding,
- the analog to digital conversions of the charge and the time signals of the hit channels : two 14-bit ADC per group (12 bits used),
- the buffering (FIFO) of the digital results.

Each board provides an analog multiplicity level of 1 mA per channel. These signals are discriminated by the trigger system to produce, within much less than 200ns, the level 1 trigger signal (STOP) which keeps all the electronic channels as they stand: the time integrator is stopped and the charge integrator value is maintained. After a delay of about 5μs the level 2 trigger signal (TRIGGER) starts the digital conversions
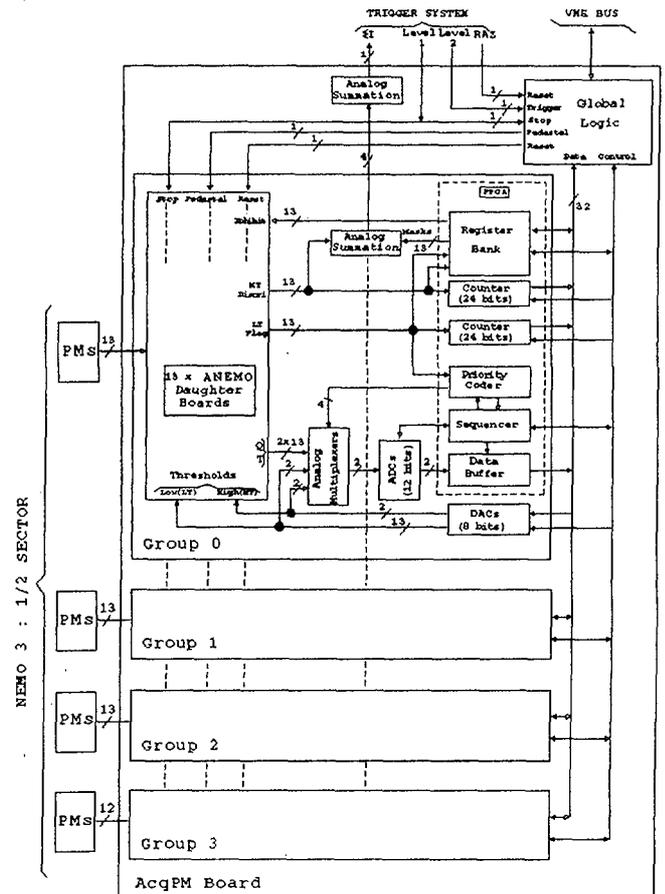

Figure 7. Calorimeter Board Block-Diagram.

The charge and the time conversion delays per channel in each group are about 6μs. For the pedestal or the calibration measurements all the channels are converted in less than 100μs

The digital functions of each group are performed by one Xilinx Spartan XCS20 FPGA.

The power dissipation of a fully equipped board is 110W and the cost, without analog daughter boards, is 2000 Euros.

VI. TEST SYSTEM

To debug and qualify the calorimeter electronics a test system has been developed. The test hardware is implemented as 2 VME modules:

- based upon the design of the calibration pulser of the ATLAS calorimeter [4], the pulse generator module provides 32 signals as close as possible to the real input signals : rise time of 6 ns, exponential decay with time constant of 35 ns, dynamic range from less than 0.1 pC to 1.5 nC, linearity better than 0.1%.
- the sequencer module provides trigger-like signals, particularly a very stable signal STOP with a jitter better than 100 ps and a range of 8 steps from 25 ns to 200 ns.

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The control of the test modules, the control and the readout of the boards under test and the processing of the measurements are performed by a Macintosh computer which runs a powerful user interface set of routines written in LAL-Orsay [5].

VII. PERFORMANCES

The energy measurements resolution is better than 2.4×10^{-4} of 12 MeV full range. Figure 8 shows the charge integral nonlinearity graph for the full range. The energy differential nonlinearity is computed as the difference in counts in any of the channels from the average counts in all the channels and expressed as the percentage of the average counts. It is lesser than $\pm$ 1/4 lsb.

The time measurement resolution is 50 ps FWHM of 200 ns full range. The time relative nonlinearity is better than 0.1%.

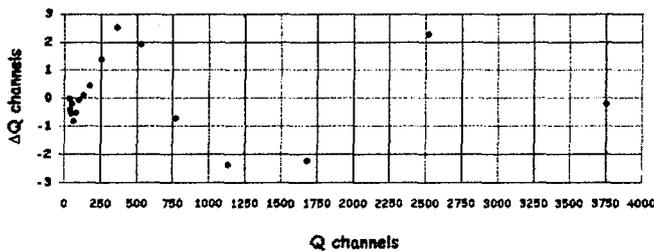Errors are computed applying least-squares analysis.

Figure 8. Charge integral nonlinearity.

The analog multiplicity level delay is less than 10 ns and its rise time jitter is 100 ps FWHM.

VIII. CONCLUSIONS

The calorimeter electronics fulfills the energy and timing measurement requirements over the 2000 channels of the NEMO experiment. The implementation as one small SMD daughter board per channel and as one VME board per 1/2 sector of the experiment apparatus provides a cost-effective realization. This complete electronics occupies a volume of about 1/2 m^3 and dissipates 4.5 kW. Its setting up at the experiment place is in progress.

IX. ACKNOWLEDGMENTS

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X. REFERENCES

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