Charge-Collection Efficiency of GaAs Field Effect Transistors Fabricated with a Low-Temperature Grown Buffer Layer: Dependence on Charge Deposition Profile

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I. INTRODUCTION

Significant advances in our understanding of the charge-collection processes of GaAs FETs, and their role in single-event phenomena, have been achieved in recent years [1-11]. The 1989 observation of charge collection in GaAs FETs in excess of that deposited by the ion [1,2], coupled with the measurement of anomalously low SEU thresholds for GaAs circuits [5], has sparked a renewed interest in the charge-collection processes of these devices. Recently, the implementation of low-temperature grown (LT) GaAs buffer layers has been found to inhibit charge-enhancement process in GaAs devices [9-11], leading to a significant reduction in their SEU susceptibility [12]. The LT GaAs results, in particular, illustrate that enhanced charge collection is a primary contributor to the poor SEU performance of non-LT GaAs FET-based ICs.

Despite the recent advances in our understanding of the charge-collection processes in GaAs devices, much remains to be understood about the complex physics of carrier transport and enhancement in LT GaAs devices, and their relationship to SEU. In this paper we present two-dimensional computer simulation results that interrogate the dependence of the charge-collection and charge-enhancement phenomena in LT GaAs MESFETs on the depth profile of the deposited carriers.

A primary advantage of computer simulation is the ability to perform (computer) experiments that are not experimentally accessible. At RADECS97 [13] we introduced the concept of "ion-track segments" as a useful tool for investigating the complex physics of carrier transport and collection in semiconductor devices. By varying the location of the injected carriers in ways that are difficult to reproduce experimentally, different contributions to the charge-collection processes can be emphasized, permitting more detailed evaluation than is possible with conventional (complete-track) simulations. In our initial study of this type on conventional GaAs MESFETs [13], the results were particularly enlightening.

While this investigation is primarily concerned with elucidating the mechanisms of charge collection and enhancement in LT GaAs FETs, is also has important practical implications. One such implication is the unexpected observation of proton- and neutron-induced upsets in LT GaAs devices [14]. SEUs from protons and neutrons are largely a consequence of nuclear reactions which can occur at any point along the initiating particle's trajectory, giving rise to localized charge deposition that in many ways is analogous to the idealized ion track segments utilized here. The location of the nuclear reaction and the trajectories of the resultant particles may have a significant influence on the charge-collection efficiency and, consequently, the probability of SEU. Also relevant is the possibility of interactions with heavy ions having large angles of incidence. In such events the ionizing particle may miss the "active" region of the device entirely, but may still deposit significant charge into the device substrate. Our initial study on ion track segments suggests that such events are expected to have a significant effect on the SEU rate in non-LT GaAs MESFETs [13]. The present study represents a first look at the possible role of such processes in LT GaAs FETs.

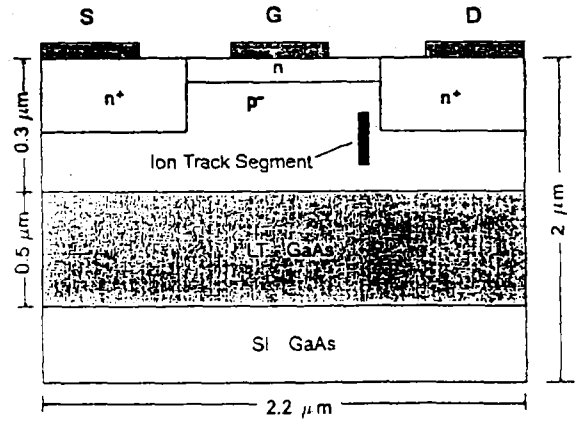

Figure 1. Schematic diagram of the 0.8 μm gate length n-channel LT GaAs MESFET modeled in this study showing schematic representation of an ion track segment.

II. COMPUTER SIMULATION

Two dimensional computer simulations were performed on the transport properties on enhancement-mode n-channel MESFETs following interaction with ionizing radiation utilizing the SILVACO code

ATLAS. A cross section of the device under analysis is illustrated in fig. 1, together with an example of an ion track segment. For the purposes of this study the ion track segments represent some portion of a complete ion track, the location of which is varied to interrogate the effects of charge deposited at different depths and lateral dimensions in a device. The basic MESFET model is patterned after the 0.8 μm gate length enhancement-mode devices fabricated by Vitesse Semiconductor, the radiation-induced dynamics of which have been investigated recently through both experimental and simulation studies [3, 6]. The 0.5 μm thick LT GaAs buffer layer is located 0.3 μm beneath the surface of the device, and is bounded on top and bottom by 100 Å thick AlAs layers (not indicated in fig. 1). More details of the simulation code will be given in the full paper.

Earlier charge-collection simulations of LT GaAs FETs have modeled the LT buffer layer by assuming a 1 ps carrier recombination time [11]. Recent experimental results suggest, however, that the carrier lifetime in the current technology is longer than the 1 ps previously assumed [15]. Contributions from both the material growth and processing are expected to effect the carrier lifetime in the LT buffer of fabricated devices, but more study in this area is required before any definitive conclusions can be made. In the present investigation, to be more in accord with the available experimental data, we utilize a carrier recombination time of 3.5 ps in the LT material. Simulations also have been performed for 1 ps lifetime material; the qualitative trends are in agreement with those presented here, however, the CCE is somewhat smaller for all segment depths.

The ion track is modeled as a 0.04 μm wide column of charge with 8×10^{18} carriers/cm^3 at t = 0. For the results presented in this summary the ion track is introduced at normal incidence to the surface in the region of the device between the gate and drain electrodes. The ion track segments are introduced as 0.2 μm long segments of the complete track at varying depths in the device. A schematic representation of one such ion track segment is shown in fig. 1. Additional simulations have been performed as a function of the lateral location of the track segments, and also for complete ion tracks at large angles of incidence. Results of those studies will be presented in full paper.

III. Simulation Results

Ion track segments can be a useful tool in investigating the mechanisms of charge collection in GaAs FETs and other devices. Figure 2a illustrates the dependence of the charge-collection efficiency on the depth of the deposited charge segment. In this figure the depths noted are the average depths for the 0.2 μm

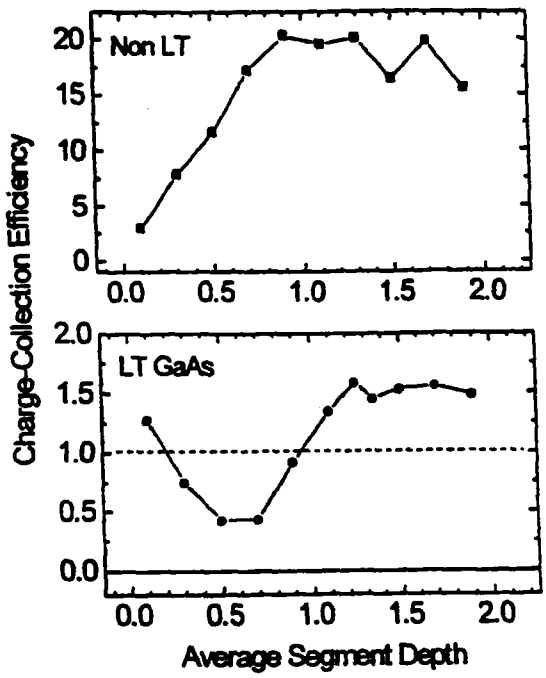

Figure 2. Drain charge-collection efficiency calculated as a function of the segment depth for 0.2 μm ion track segments for LT GaAs and conventional (non LT) MESFET. $V_D = 2.0$ V; $V_G = 0.05$ V.

long track segments. As is evident, the charge collection efficiency is greatest for charge deposited in the substrate of the device, and smallest for charge deposited near the surface. An analysis and detailed discussion of the data that contributes to the individual data points of fig. 2a is presented in [13].

Given the current understanding of the charge collection processes in GaAs FETs, and particularly the significance of charge-enhancement phenomena, this result is not especially surprising. However, it should be noted that the behavior observed is precisely the opposite of that predicted for conventional charge-collection models, such as the rectangular-parallel-piped model. Figure 2b shows the behavior of the ion track segments for the LT GaAs device. Recall that the LT GaAs buffer extends from 0.3 μm to 0.8 μm, and note that the CCE for the LT GaAs device is roughly an order of magnitude smaller than that of the non-LT device. These data illustrate that charge collection is minimized for carriers deposited directly in the LT buffer (as expected), and that the CCE curve exhibits a maximum for charge deposited near the surface of the device. The surprising aspect of the data of fig. 2b is the resurgence of the CCE curve for charge deposition below the LT GaAs layer: the CCE exhibits its maximum value for

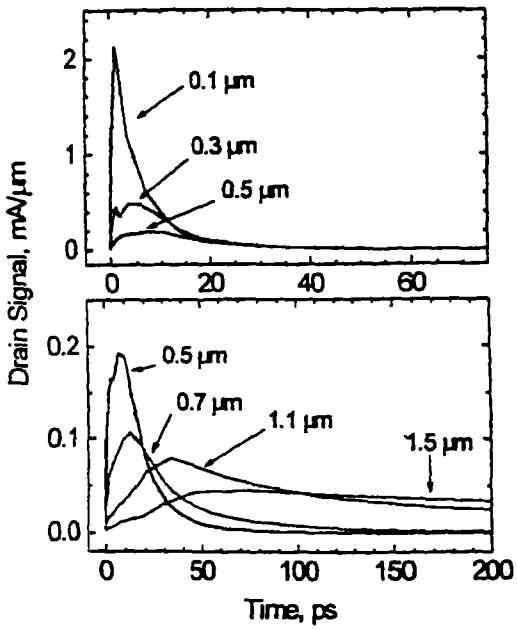

Figure 3. Drain current transients calculated as a function of the average segment depth for 0.2 μm ion track segments corresponding to the data of fig. 2b. $V_D = 2.0$ V; $V_G = 0.05$ V.

carrier deposition below 1.2 μm! The origin of this unexpected result is revealed by investigating the dynamics of the charge-collection process, which are illustrated in fig. 3.

The data of fig. 3 illustrate the evolution in the shape of the charge-collection transients as the depth of carrier deposition is varied. For a charge track segment located in the top 0.2 μm of the device there is a rapid, intense burst of collected charge that quickly decays to zero. This initial burst of collected charge is associated primarily with the direct collection of the deposited carriers (although there is some charge enhancement as well). For progressively deeper carrier deposition, the "prompt" contribution becomes less significant, the signal peak is delayed in time, and the signal decay becomes progressively slower. It is evident from these data that, although the charge-collection efficiencies for carrier deposition above and below the LT buffer are of similar magnitude (*cf.*, fig 2b), the mechanisms of charge collection in the two cases are decidedly different.

Detailed insight into this result is obtained through investigation of the temporal evolution of the carrier densities and potentials in the device for the different ion track segments. Space constraints, however, do not permit presentation of more than a single example in this summary. Figure 4 shows the electron density contours and corresponding current vectors for ion track segments of three different

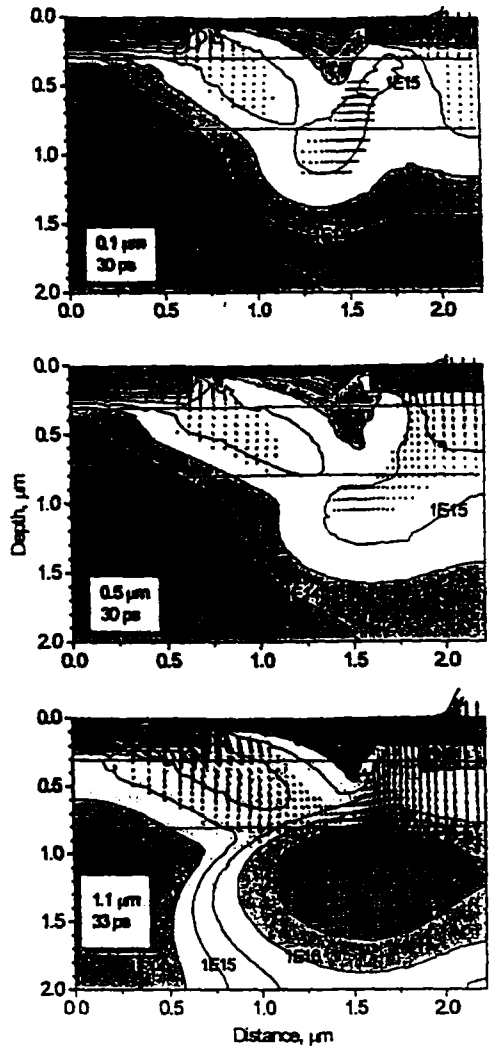

Figure 4. Electron density contour plots for three different track segments 30 ps after the ionizing event. The solid horizontal lines indicate the boundaries of the LT GaAs buffer layer.

depths 30 ps after the ionizing event. For this time step the "prompt" collection of deposited charge is effectively complete (*cf.*, fig. 3a) and, for the track segments centered at 0.1 μm and 0.5 μm, the residual current amplitude is associated with a small "bipolar-like" charge-enhancement process. For the 1.1 μm deposition, however, significant current associated with this "bipolar-like" process is evident. This example suggests that charge deposition below the LT buffer layer is more efficient in initiating the bipolar-like gain process. Investigation of the corresponding potential contour diagrams reveals the the deeper deposition has a more significant effect on the fields in the device, giving rise to more significant and persistent barrier lowering at the source/substrate junction. A more detailed discussion of these issues will be presented in the full paper.

IV. CONCLUSIONS

The results presented here reveal a surprising dependence of the charge-collection efficiency of LT GaAs FETs on the depth profile of the deposited charge. Investigation of the temporal dependence of the signal amplitude, carrier density contours, and potential contours reveals different mechanisms for charge collection arising from carriers deposited above and below the LT GaAs buffer layer, respectively. In particular, carriers deposited below the LT GaAs buffer layer dissipate slowly and give rise to a persistent charge collection that is associated with a bipolar-like gain process. These results may be of significance in understanding the occurrence of single-event upsets from protons, neutrons, and large-angle, glancing heavy-ion strikes.

The results presented here complement laser-induced charge-collection measurements on LT GaAs HFETs performed as a function of the laser pulse wavelength [16]. Variation of the laser pulse wavelength changes the charge deposition profile in the device by changing the 1/e optical penetration depth. The ion-track segment results presented here provide insight into those measurements, an analysis of which will be presented in the full paper.

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