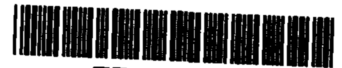
FR0203837
INIS-FR--1132

Optimized Stacked RADFETs for milli-rad Dose Measurement

Barry O'Connell, Dr. Bill Lane - NMRC-National Microelectronics Research Centre - NMRC, Cork, Ireland.

Dr. Ali Mohammadzadeh, ESA-ESTEC, Noordwijk, NL.

Abstract

This paper details the improvements in the design of stacked RADFETs for increased radiation sensitivity. In [1], [2] & [3] the concept of connecting RADFET devices in series - stacking - has been presented. The issue of high read-out voltage has been shown to be a draw-back. It is the body (bulk) effect factor that is responsible for the increased overall stack Threshold voltage (V_T), which is greater than the sum of the individual devices V_T. From extensive process & device simulation and resultant circuit simulation, modified stack structures have been proposed and designed. New and exciting results of lower initial (pre-irradiation) output voltage as well as increased radiation sensitivity will be presented.

Introduction

The concept of the RADFET [4] as a radiation dosimeter is well known. Radiation induced charge in the optimally grown thermal oxide changes device V_T. The amount of V_T change is in proportion to the amount of accumulated total ionising dose. Read-out of V_T is by the Reader Circuit measurement schematically described in figure 1a. Processing improvements of RADFET devices has enabled radiation sensitivity values of >7mV/rad [1], [5] to be achieved. A design approach [2] has demonstrated radiation sensitivities of >85mV/rad. For medical, nuclear facility personnel and other applications, where < milli-rad doses are required to be measured, radiation sensitivity of the order of hundreds of mV/rad are required. The Vo of 4 stacked devices is shown in equation 1, which shows the dependence on W/L as well as other device parameters.

$$Vo = -4V_{T0} + CURR3 + \gamma(\sqrt{-3V_{T0} + CURR3 - \Phi_B} - \sqrt{\Phi_B}) + \sqrt{\frac{2I_{SD4}\left(1 + \frac{\gamma_4}{2\sqrt{-\Phi_B - 3V_{T0} + CURR3}}\right)}{\frac{W_4}{L_4}\mu_4 Cox_4}} \qquad \text{Equation 1}$$

where the CURR term is similar to the final term of equation1 - it is an iterative current dependent term in the stacked device equations, V_{T0} is the single device V_T with V_{BS}=0V, γ is the body-effect factor $= \frac{\sqrt{2\varepsilon_s q N_D}}{Cox}$, ε_s is silicon permittivity, q is electronic charge, N_D is substrate doping, Cox is oxide capacitance, Φ_B is bulk potential, I_{SD} is source-drain current.

Figure 1b shows a circuit schematic of stacked devices. The drain and gate of each device are connected. The bulk can be tied to the source of the first device in the stack (V_{BS1}=0V). Alternately the bulk terminal can be separated from the source of the first device and a bulk voltage may be applied in order to control the Vo, as shown in figure 1b [6]. The aim of this work is to achieve milli-rad dose detection capability with a low (<20V) initial Vo. Simulation work [7] has shown that changing the transistor device geometry Width/Length W/L has a major effect on the initial Vo and radiation sensitivity of the stacked devices. The source-drain current dependence on W/L is shown in equation 2 [8] for a single device in strong inversion, where μ is carrier mobility, $\delta = \frac{\gamma}{2\sqrt{-\Phi_B - V_{SB}}}$

$$I_{SD} = \frac{W/L\mu Cox[V_S - V_D + V_T]^2}{2(1+\delta)} \qquad \text{Equation 2}$$

For a single device, larger W/L means smaller Vs term for a constant current. Using HSPICE level3, the effect of varying W/L on stacked structure Vo is analysed in the experimental section as well as the effect on overall radiation sensitivity.

Experiment

The effect of varying W/L on stacked structure Vo is shown in figure 2. Increasing device W and decreasing L has the effect of decreasing magnitude of Vo and increasing radiation sensitivity. As well as magnitude of Vo,

radiation sensitivity is of paramount importance to the suitability of using stacked RADFET devices in applications that require high radiation sensitivity. The modelling of radiation sensitivity has been achieved by changing device V_T from pre-irradiation values in SPICE to values that correspond to a known amount of radiation. This is possible as the single device radiation sensitivity is well known and not affected by device W/L. Different W/L configurations are thus analysed.

A new layout using the above ideas has been designed and masks have been fabricated. Fabricated RADFET devices of 4kÅ and 9.2kÅ implanted gate oxide are almost at completion and will be electrically tested to verify the simulated results. After electrical testing, the stacked devices will be irradiated with Co60 gamma-rays. A number of different W/L configurations have been designed and will be fabricated in to RADFET stacked devices; up to 38 devices of W=600μm, W=1530μm and W=3060μm with L varying from 17 to 11μm. All chip sizes in the new layout are either 1*1mm, 2*1mm or 2*2mm. Figure 3 shows 12 stacked 1530/13μm RADFET devices. The double drain W=3060μm stacked devices as well as increasing radiation sensitivity and reducing Vo magnitude should also result in lower device noise [9]. This should result in a larger Signal/Noise ratio enabling a lower minimum detectable radiation dose to be measured. Results will be presented of stacked device Vo improvement, radiation sensitivity increase, read-time drift, fading, device noise & temperature effects and calculated minimum detectable dose.

References

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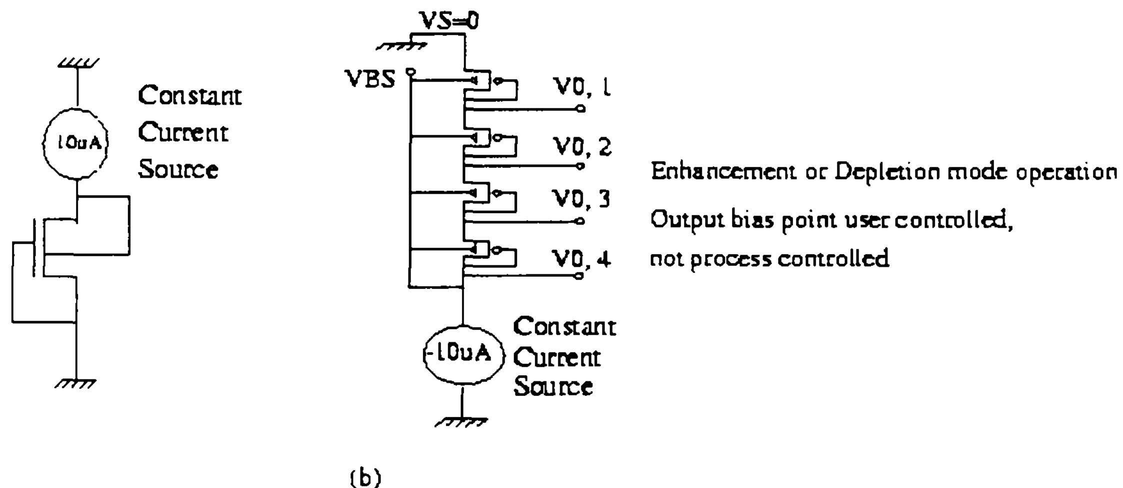

Figure 1. Circuit schematic of (a) single device in Reader Circuit configuration and (b) in stacked device configuration.

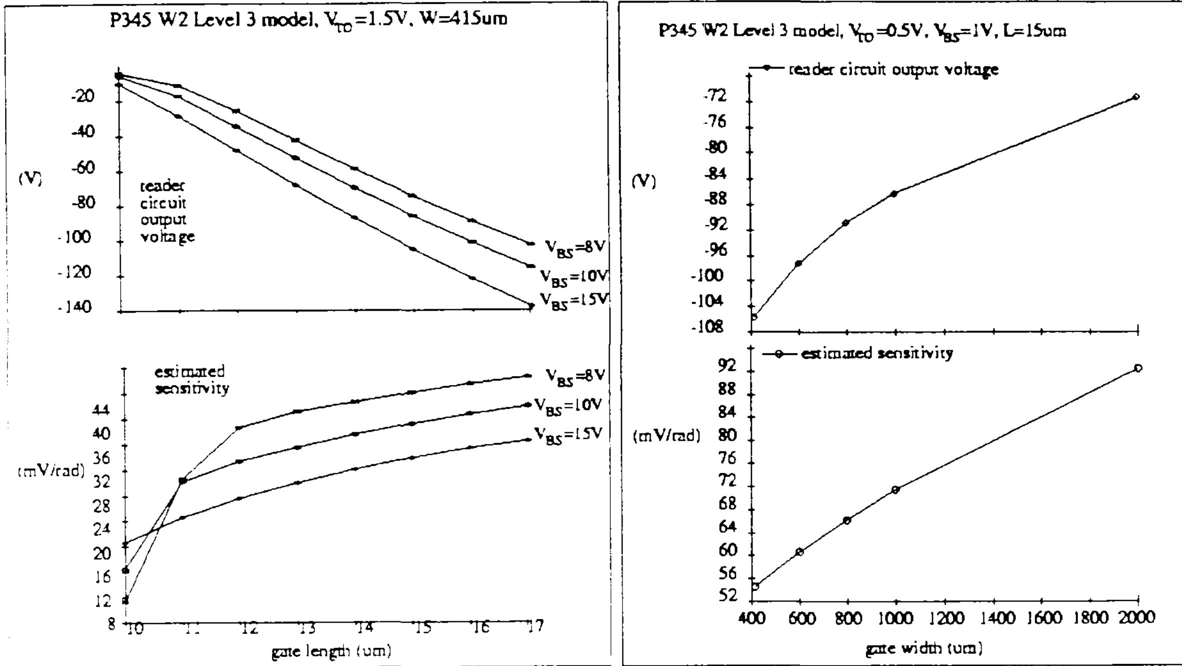

Figure 2. Modelled Effect of variation of device (a) W on Vo magnitude and radiation sensitivity
(b) L on Vo magnitude and radiation sensitivity

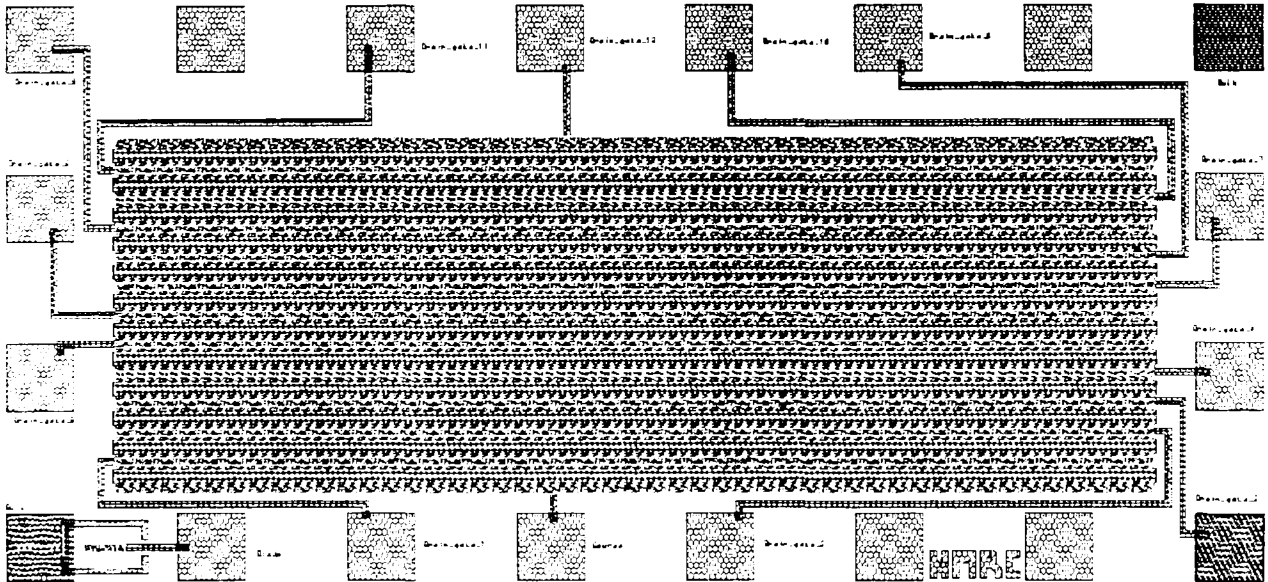

Figure 3. Layout of 12 stacked 1530/13µm W/L RADFET devices. Chip size is 2*1mm.