Relationship between Single-Event Upset Immunity and Fabrication Processes of Recent Memories

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Abstract

Single-Event upset (SEU) immunity for commercial devices were evaluated by irradiation tests using high-energy heavy ions. We show test results and describe the relationship between observed SEU and structures / fabrication processes.

I. INTRODUCTION

Recently, the space application of commercial memory devices have been received considerable attention in connection with the reduction of the cost and weight of spacecrafts without lowering their performance. In the present study, we have evaluated single-event upset (SEU) tolerance of recent commercial memory devices using high energy heavy ions in order to find relationship between SEU rate and their fabrication process [1].

II. EXPERIMENTAL

The samples used for this SEU tests were commercial 16Mbit DRAMs, 64Mbit DRAMs, 1Mbit SRAMs and 4Mbit SRAMs. 64Mbit DRAMs consisted of 2 different generation devices, i.e. the second and third generation. Difference of generation is smaller memory cell size and structure. 16Mbit DRAMs were from 2 different device manufacturers. These samples were irradiated with several kinds of heavy ions, such as 120MeV-Ne^{6+}, 175MeV-Ar^{8+} and 450MeV-Xe^{23+} obtained from an AVF cyclotron at JAERI Takasaki. In the SEU experiments, the number of memory bits in which upset occurred by ion irradiation and the ion fluence irradiated to the samples were measured to calculate the SEU cross-sections. From the SEU data acquired under several irradiation conditions, we obtained the SEU cross-section as a function of linear energy transfer (LET) in silicon.

III. RESULTS AND DISCUSSION

Figure 1, 2 and 3 shows memory cell cross-section of 16Mbit, 64Mbit(2nd) and 64Mbit(3rd) DRAM. Table 1 shows process technology parameters for 16Mbit and 64Mbit DRAMs [2],[3],[4]. Memory cell size of 16MbitDRAM is bigger than that of 64Mbit DRAM. For the 3rd generation of 64MbitDRAM, the memory cell size was almost 2/3 of the 2nd generation, however the memory cell capacitance was not changed because of hemi-spherical-grained structure on the surface of the memory cell electrode. From these data it was expected that saturated cross-section for the 3rd generation would be smaller than the 2nd generation, whereas threshold LET would not be changed between the 2nd and 3rd generation 64MbitDRAM. The dependence of the SEU cross-section as a function of LET for several devices is shown in figure 4. The threshold LET and the saturated cross-section were derived from the SEU cross-section vs. LET curve for each sample and the values of them are shown in table 2 [5]. As a comparison of the test results for two 64Mbit DRAMs, almost the same values were obtained for the saturated cross-sections.

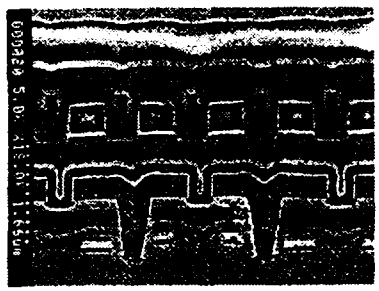

Figure 1 : Memory cell cross-section of 16Mbit DRAM [2]

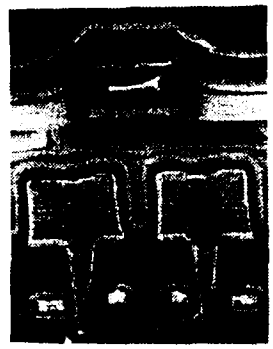

Figure 2 : Memory cell cross-section of 2nd generation 64Mbit DRAM [3]

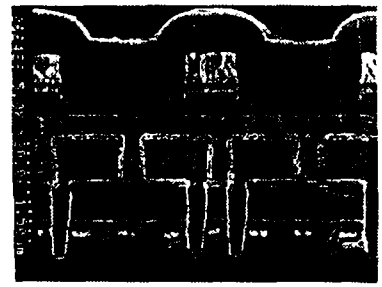

Figure 3. Memory cell cross-section of 3rd generation 64Mbit DRAM [4]

Table 1. 16Mbit and 64Mbit DRAM process technology [2],[3],[4]

		16Mbit DRAM	64MbitDRAM	
		2nd generation	2nd generation	3rd generation
Structure		N well CMOS 2 aluminum layer	3 stacked well CMOS 2 aluminum layer	3 stacked well CMOS 1 aluminum layer/ 1 tungsten layer
Technology rule		0.45μ•	0.32μ•	0.28v•
Channel length	PMOS	0.9μ•	0.7μ•	0.51μ•
	NMOS	0.7μ•	0.5μ•	0.43μ•
Gate oxide layer		140A	110A	100A
Memory cell	size	2.48x1.24=3.075μm^2	0.778x1.58=1.25μm^2	0.65x1.3=0.84μm^2
	structure	Stack (Capacitor Over Bit-line)	Stack (Capacitor Over Bit-line)	Stack(Capacitor Over Bit-line+ Hemi-Spherical Grain Si)
	Capacity	27fF	25fF	25fF
Supply voltage		5.0±0.5V	3.3±0.3V	3.3±0.3V

However, the threshold LET for these devices were considerably different, i.e., at about 2 times. This result may be attributed to the difference of the process technology and the structure between these devices. In the 2nd generation, only aluminum layer was used. But the 3rd generation was changed to the aluminum layer and tungsten layer. It was thought that increased threshold LET for the 3rd generation was caused by the difference of the material This result also suggests that the SEU rate is not predictable with old data for new process technology even it the manufacturer is the same [6].

Both of the 16Mbit DRAM(NEC) and 64Mbit DRAMs were manufactured by the same manufacturer. From SEU test data, it was indicated that the ratio of the saturated cross-section was consisted with the memory cell size as expected. It is known that the critical charge depends on the cell capacitance. From the process data, the memory cell capacitance of the 64Mbit DRAMs is smaller than that of the 16Mbit DRAMs. Thus, difference of the threshold LET is expected between these two devices, which is consistent with the experimental result.

IV. CONCLUSION

We have evaluated single-event upset (SEU) tolerance of recent commercial memory devices using high energy heavy ions in order to find relationship between SEU rate and their fabrication process. It was revealed that the change of the process parameter gives much effect for the SEU rate of the devices.

REFERENCES

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Table 2 Threshold LET and Saturated Cross section

	Threshold LET (MeV/(mg/cm^2))	Saturated Cross section (cm^2/bit)
1Mbit SRAM	5.6	$3.3x10^{-7}$
4Mbit SRAM	1.3	$3.0x10^{-7}$
16Mbit DRAM Toshiba	4.2	$2.1x10^{-8}$
16Mbit DRAM NEC	4.1	$1.6x10^{-7}$
64Mbit DRAM 2nd generation	2.4	$3.0x10^{-8}$
64Mbit DRAM 3rd generation	5.4	$3.9x10^{-8}$

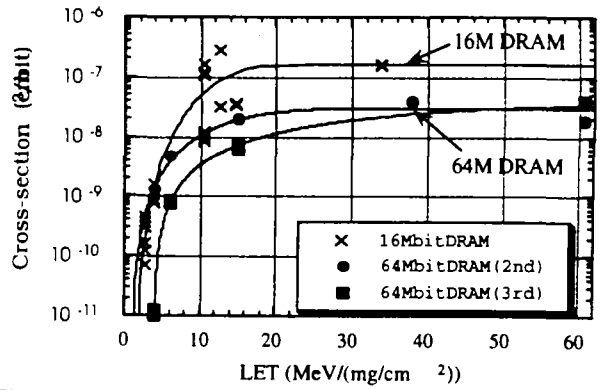

Figure 4 LET vs. Cross section of memory ICs