Quantification, Modelling and Design for Signal History Dependent Effects in Mixed-Signal SOI/SOS Circuits

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Introduction

This paper deals with how the radiation hardness of mixed signal SOI/SOS CMOS circuits is taken into account at both architectural terms as well as in the transistor level cell designs. The primary issue is to deal with divergent transistor threshold shifts, and to understand the effects of large amplitude non-stationary signals on analogue cell behaviour.

Threshold Voltage Divergence

Most foundries give limited data for threshold shift measured at the bias levels encountered at the normal logic levels. However, the analogue designer must consider all possible values of bias within the supply limitations [1]. Figure 1 shows typical data for a mature process measured specifically for this design. Hence, two initially identical devices operating under differing biases will become unmatched after radiation. This can cause failure in many types of circuit cells, particularly where extensive cascoding is used to achieve high gain, or to ameliorate floating body effects in and SOI process. Difficulties arise when bias networks are used wherein reference voltages are derived from transistors with different gate bias values. This problem must be handled in terms of carefully designed biasing networks [2]. A special SPICE based simulation tool has been used for our designs in which the radiation induced operating point evolution of analogue circuits can be simulated. A simple model for trapping [3] is incorporated into a simulation result file processor to update iterative simulation conditions.

Non-Stationary Signal Effects

In many classes of analogue design, signals may often be consider "small" in comparison with the effective transistor bias values; hence if two transistors have equal bias, but only one sees a very small time varying signal, the radiation induced threshold shift will be essentially equal, and normal analogue matching philosophies may be adopted. However, in data conversion circuits, signals at comparator inputs etc may have quite large AC as well as DC components. The implications for device matching are not clear. One could postulate that if the input to one transistor in a matched pair is equal to the time averaged value of the input to the other, then again essentially equal radiation effects could be observed.

To investigate this hypothesis, arrays of matched devices were fabricated and biased during exposure to a Co60 γ source. The arrangement is shown in figure 2. One device of a pair is has a signal on its gate derived from a signal generator, and the other is biased from a low-pass filtered version of the generator output, i.e., the time averaged value. Relays were installed on the test board to allow circuit reconfiguration for measurement of transistor Vt at periodic intervals during exposure. Typical results with 50% duty cycle 0-4V pulse inputs are shown in figure 3. It is obvious that for the large signals typical in data conversion applications, the assumption that the radiation effects with a large AC bias component are not equivalent to those observed with the time averaged DC value present. Clearly, analogue circuits, particularly single ended signal paths dependent on matching, cannot be designed from this premise, and other architectural approaches must be investigated.

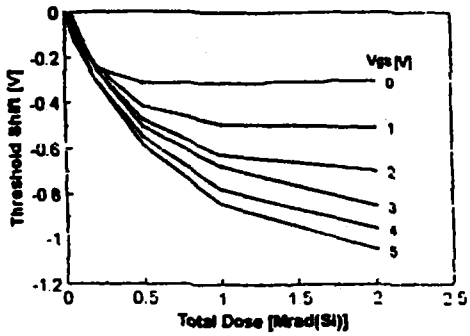

Figure 1 – Vt vs dose vs Vgs

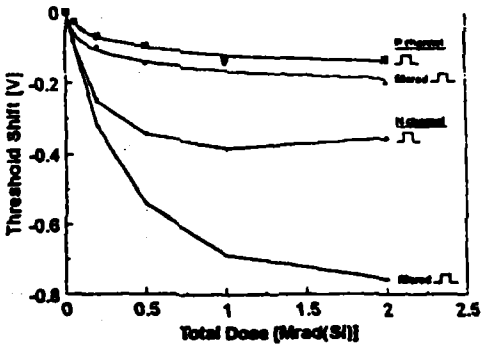

Figure 3 – Vt vs Dose for Vgs AC and DC Vgs

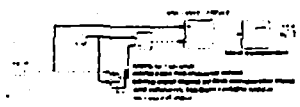

Figure 5 – Behavioural Model for Signal History Dependent Comparator Offset

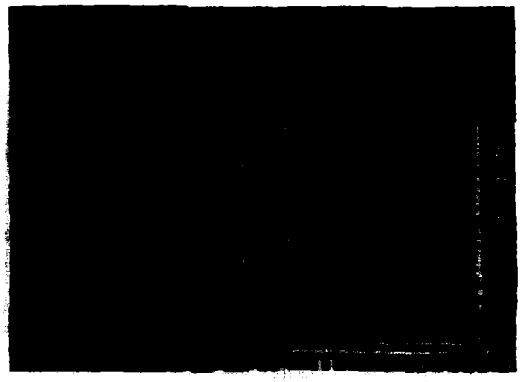

Figure 7 – 7 Bit Flash A/D Chip in 1.5u SOS

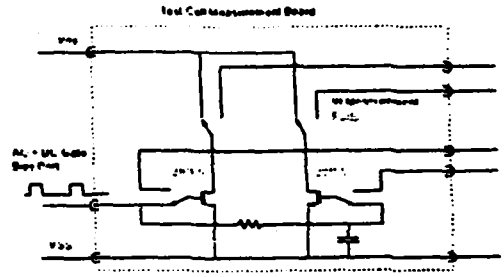

Figure 2 – Test Board for AC Vgs vs Dose Tests

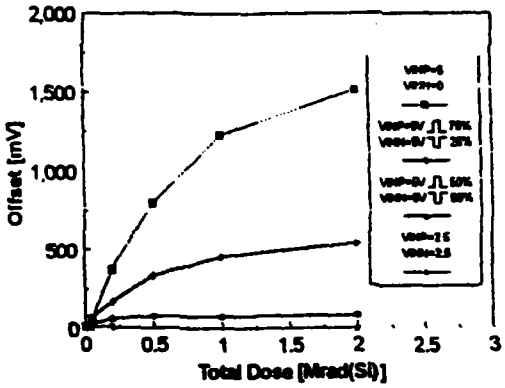

Figure 4 – Input Referred Offset of Differential Input Amplifier for Various Input Signals During Irradiation

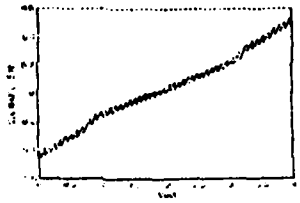

Figure 6 MATLAB Simulation of Error in 6 Bit Flash A/D

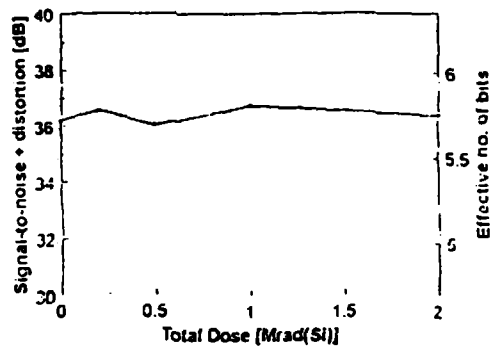

Figure 8 – A/D Performance with Static +/- 0.5V Unbalanced Input Applied

Signal History Effects

Signal history dependence is also something that is quite architecturally dependent. In many analogue applications the use of fully differential architectures, possible with virtual earth configurations, means that some critical transistors experience equal bias conditions, and hence there is minimal divergence of threshold during radiation. Thus no radiation related offset is a created. However, in analogue to digital conversion circuits, the decision processes often demand that amplifiers and comparators cannot be assumed to have ideally balanced or virtual earth input conditions. Large differential mode signals can be present on initially balanced circuit cell inputs for as long as a signal has a particular value. This is even true in differential architectures. Hence transistor stresses become subject of the history of the signal presented to the circuit, and consequently, resulting input referred offsets are also dependent on history.

This point is demonstrated experimentally by examining the input referred offset of an amplifier cell before and after radiation for different input signal history conditions. A classical amplifier with a P-channel differential pair input configuration was exposed to radiation whilst the inputs biased in different ways. Some sample had steady DC values of VDD/2 applied to both input ports; other samples had one input pulled high and one low; other samples had time varying signals of differing magnitudes applied to the inputs. Figure 4 shows that under extreme differential bias conditions during exposure, very large input referred offsets can arise; in the results presented, values of more than 1V are observed.

Behavioural Modelling of System Sensitivity

From this study, behavioural models of the comparator function were developed which take into account the signal history and a specified radiation dose (figure 5). These were then used in MATLAB to show how different A/D architectures have different sensitivities to such signal history dependencies. Non-idealities such as linearity reduced dynamic range, global offsets and missing code levels are predicted in various degrees for various architectures. Figure 6 shows typical results from simulation of a 6 bit flash A/D. Feed-forward type architectures are shown to be particularly sensitive.

A/D Circuit Design

A 7 bit flash A/D and several primitive analogue cells were designed and fabricated in floating body SOS CMOS using the data and ideas mentioned here. New circuit level tricks are used to equalise the unbalanced signal history components, and then to remove the residual offset terms remaining by calibration techniques. Previously reported A/D designs [4,5] have used auto-zero techniques in single ended flash converters. Here, using fully differential architectures, chopping minimises the influence of signal history in a time-averaged sense. Note that this must be applied to both the signal path and any reference level path since the reference values applied to a comparator in the decision process may also be strongly unbalanced, depending on the particular position of the tapping on the reference ladder structure. This approach is shown to reduce the offset terms to the levels capable of being handled by auto-zero type circuits.

Results and Conclusions

The fabricated circuit is shown in figure 7. Despite being constructed in a digital floating body technology with poor transistor performance, the converter yields 5.5 bits at 2Ms/s. Radiation testing under signal bias conditions shows minimal change in behaviour after more than 20Mrad(Si) with no visible influence of unbalanced input signal history. New bias techniques and differential architectures with averaging of asymmetric signal history maintain internal circuit operating conditions despite these high dose levels.

References

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