A COTS-based Single Board Radiation-Hardened Computer for Space Applications

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A. ABSTRACT

There is great community interest in the ability to use COTS technology in radiation environments. Space Electronics, Inc. has developed a high performance COTS-based radiation hardened computer. COTS approaches were selected for both hardware and software. Through parts testing, selection and packaging, all requirements have been met without parts or process development. Reliability, total ionizing dose and single event performance are attractive. The characteristics, performance and radiation resistance of the single board computer will be presented.

B. INTRODUCTION

Spaceborne computers, for both strategic and natural environments, have required complex and expensive solutions to the environmental issues involved. These issues involve solutions to mechanical and thermal vacuum conditions, but particularly to the radiation environment. In postulating its approach to this product area, Space Electronics Inc. (SEi) early-on decided to pursue a COTS (Commercial Off The Shelf) hardware and software solution to minimize cost, maximize ease of use and reduce development lead time. This paper will report on the achievement of these goals. Initially, the latest version of the Intel 486DX2 CPU was tested and found to have acceptable radiation hardness properties when assembled into the SEi RAD-PAK® package. This allows use, in Space, of the world-standard Intel architecture and CISC (Complex Instruction Set Computer) instruction set VXWorks, a well established, readily available and widely understood OS (Operating System), was selected, supporting ease of both computer and application software development. As an established radiation test supplier, SEi was able to complete parts selection with a combination of existing rad-hard parts, selected/screened military or commercial parts and packaging of certain devices, particularly memory, in RAD-PAK® packages. No device or process development was needed or performed.

The resulting Space Electronics SB486R computer is contained on a single PWA (Printed Wire Assembly). Its initial delivered configuration is sized at 203.2(L)* 154(W)* 25.15(H) mm. A second configuration was developed to the VME 6U requirements. Weight is less than 0.8 Kg. Power is <12.5 W. The PWB (Printed Wire Board) is copper core, for thermal and structural integrity during boost and orbital missions, and includes two (2) "Q" stiffeners for shock and vibration performance improvement. The PWA has been successfully tested to 1000G/700 Hz. Shock, $0.5G^2/Hz$. Random Vibration, 25G Sinusoidal Vibration, Temperature Shock and Thermal Vacuum testing to 1E-5 Torr at orbital temperatures. Spacecraft interface is through the Amphenol M55302/168C40Y2 or the above-noted VME 6U standard. Thermal response of the SB486R is excellent, due to the copper core used in the PWB.

The significance of this work, when supported with appropriate test data confirming performance, will be found in the significant reduction of both cost and lead time for development of radiation hardened processors for Space. Future plans include modularization of the design for further reduction in lead time and improvements to existing SEU performance and architecture to allow use of this computer in long-term satellite applications.

C. THE SINGLE BOARD RADIATION-HARDENED COMPUTER

1. *Functional Description*

The SEi single board computer in the SB486R family, is represented by the Block Diagram in Figure 1.

The CPU is an Intel 486DX2 operating at 66MHz. A particular lot of Intel devices was tested, both by NASA and SEi, (Ref.) and found to have attractive SEE performance. Die from this lot were procured and mounted in SEi RAD-PAK® packages for total ionizing dose performance improvement. The resulting circuit performs to Intel electrical specifications. Glue logic is provided by a selection of inherently radiation-tolerant devices and by rad-hard FPGAs (Field Programmable Gate Arrays). These provide a considerable flexibility in system design, with respect to memory and I/O choices in particular. Power is +5VDC, 2.5A. Depending on the actual –1553 selected, 15VDC may be required.

Four SEi RAD-PAK® memory types have been successfully operated in the SB486R computer family:

- A 128Kx8 EPROM is used for BootROM.
- A 256Kx32 EEPROM is used for program storage.
- A 512Kx32 SRAM, SEU-protected, with EDAC and check-bits.
- A 128MB DRAM, SEU-protected, with EDAC and check-bits.

I/O capabilities integrated to date include:

- AC 244/245 Parallel Port.
- 16552-Compatible High Speed Dual UART.
- Telemetry Serial I/F (Customer-special I/F).
- MIL-STD-1553B I/F, presently 15V, going to 5V.
- VME Bus Interface
- CCSDS
- Ethernet, discussed but not completed

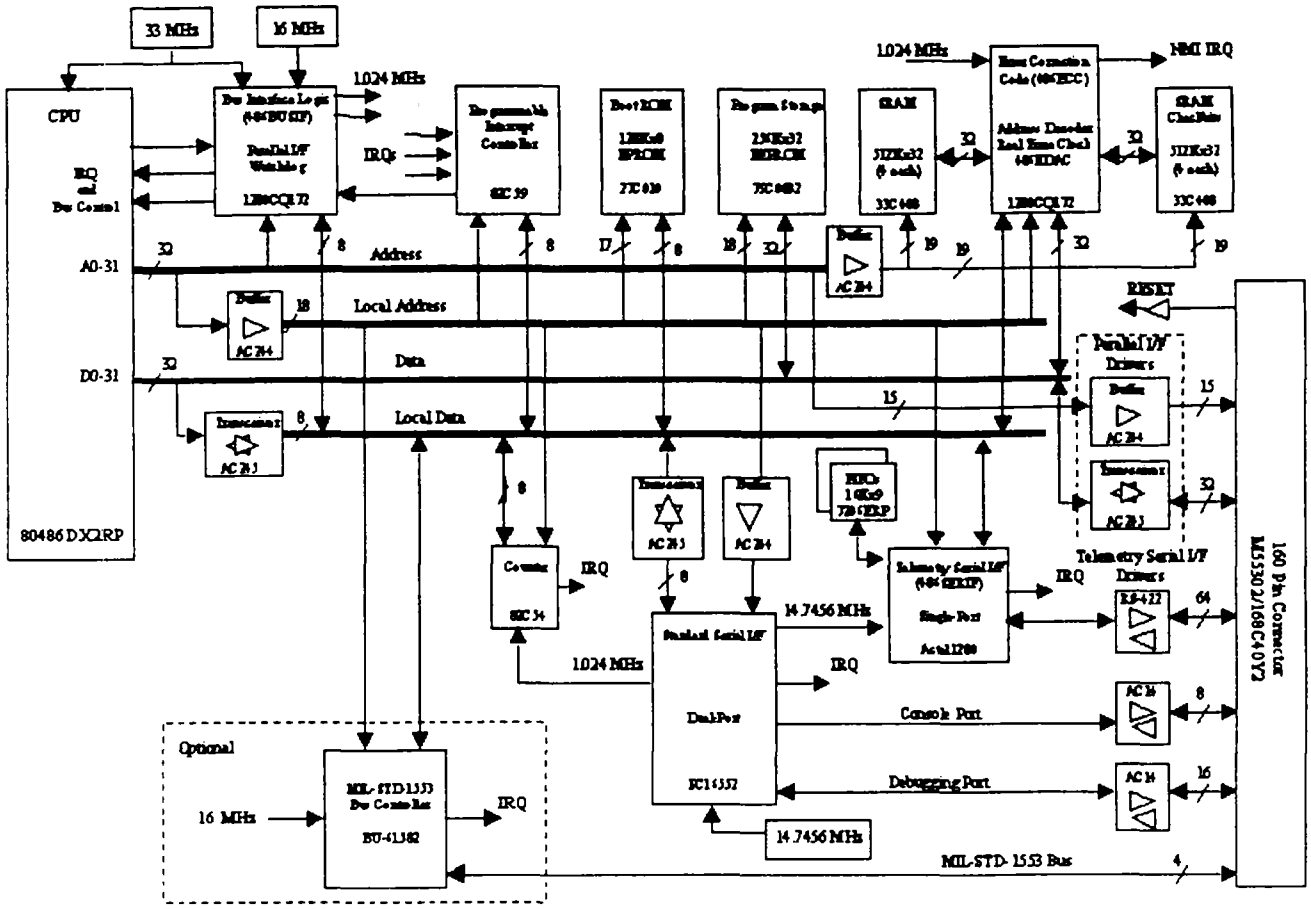

Figure 1. Single Board Radiation-Hardened Computer Block Diagram

2. *Electronic Design*

Electronic design is performed primarily in three areas: a). the overall circuit/ PWB design, b) the FPGAs used as glue in the overall PWA design and c) assembly-level functional simulation.

a) Circuit/PWB design is conventional, performed on ORCAD. At the PCB level, ORCAD is used for schematic capture and simulation. Best- and worst-case static timing analysis is done with Timing Designer from Chronology.

b) For FPGA design, SEI uses state of the art Computer Aided Engineering (CAE) tools in its FPGA and PCB design flows.

- FPGAs are designed in the VHSIC Hardware Description Language (VHDL) and simulated with ModelSim from ModelTech.
- The VHDL is synthesized into a gate-level netlist of the target FPGA using Leonardo from Exemplar. FPGA setup and hold timing as well as output timing is provided by target-specific tools.
- The netlist is then placed & routed using target-specific tools such as Altera MAX+plus II or Actel Designer. These target-specific tools also provide post-layout timing data to estimate FPGA performance. FPGA setup and hold timing as well as output timing is provided by target-specific tools.
- In addition, ModelSim can be used both pre- and post-layout to perform gate-level simulations.

c) Circuit level functional simulation is performed with chronology.

3. *Mechanical Design*

Initial design requirements are a PWA sized at 203.2(L) * 154(W) * 25.15(H) mm. Power is specified at 12.5W. The mechanical environment extreme, as will be seen below. Engineering analyses performed on the design of the SBC were structural, power and thermal. The NASA Stress Analysis (NASTRAN) program was used to perform the finite element analysis of the printed wire assembly (PWA) prior to fabrication and assembly. The comprehensive modeling results proved to be accurate in their prediction of the printed wire board's (PWBs) thermal and structural behavior.

The power and thermal analysis took into account integrated circuit (IC) package size and location, IC heat dissipation, IC duty cycle time, and the thermal conductivities of epoxy, polyimide and copper core to aluminum chassis. The actual power consumption was marginally better than the slightly conservative analytical prediction. The thermal analysis also proved to be accurate. The copper core provided an excellent thermally conductive path.

The PWB is constructed of 14 layers of polyimide with a 1.016 mm thick copper core central-layer for structural support as well as conductive heat dissipation. The 154 x 203 x 25 mm PWA weigh 0.656 Kg. It is rigidly supported on three sides and two evenly distributed central posts. The fourth side of the PWA is free of support because of the 160-pin connector interface. This connector-side of the PWB is stiffened by an aluminum bar opposite the connector.

As an established supplier of space-level components, SEi has established an assembly process of high quality and reliability. All components are inspected and traceability markings are noted on the as-built record. Integrated circuits (IC's) will have already had their leads formed by an in-house precision pneumatic press. Assembly of the SB486R will be performed exclusively in a reflow environment. The IC's are then epoxied in place. The epoxy serves as a structural bond and a thermally conductive medium to dissipate heat generated by the IC during operation. The PWB with components in place is now referred to as a PWA. The PWA is inspected by a high gain video inspection system and is then delivered to engineering for functional testing. Successful functional testing is followed by the application of conformal coat which is black-light detectable to verify 100% coverage.

The SB486R has passed all qualification and acceptance tests and is being delivered for flight test.

Table 1: Environmental Requirements

Survival	45 to + 70 °C
Operation	20 to + 65 °C
Vacuum	10^{-5} Torr
Random Vibration	0.52 g^2/Hz
Sinusoidal Vibration	25G at 15-100 Hz
Shock	1000G at 700 Hz

4. *Radiation Hardening*

All hardening strategies were considered and most were employed in the design and development of the SB486R computer. These included:

- Selection of inherently rad-hard commercial devices
- Screening of commercial lots for hardness levels
- Packaging of commercial die in the SEi RAD-PAK® shielding package
- Selection and purchase of established hardness devices
- For SEE, part-level solutions such as TMR (Triple Modular Redundancy) in FPGAs
- Finally, system-level architectural solutions such as EDAC and use of the Watchdog Timer to monitor the 486DX2 device.

Not performed was the development of radiation-hardened ICs from scratch, as unnecessary and expensive as well as outside the COTS goals.

a) Total Ionizing Dose requirements have been considered to a total dose of up to 100K Rad(si). Assuming 100K as the requirement, 14 of 48 ICs on the PWA are protected by RAD-PAK®. This technology provides an established improvement in TID protection [1,2]. With this level of protection, all ICs can meet the 100K requirement. Lower TID requirements result in a reduction of required RAD-PAK® devices to as low as four or five, depending on memory selection. A detailed presentation of hardening strategy as well as TID performance with and without RAD-PAK® is included as Figure E. This Figure is developed against the levels of a LEO orbit.

Table 2: Total Ionizing Dose

Description	Source	Part Number	TID (k) die	Life* (yrs)
CPU, 80486DX2	SEI	80486DX2RP	20[1]	34
Prog, Counter	Harris	HS9-82C54RH-8	100[2]	172
Interrupt Controller	SEI	82C59ARP	100[4]	172
Hex Schmitt Inverter	Nat'l	RM54AC14SDA	100[5]	172
Crystal Osc.	Q-Tech	QT25AC10M-X	100	172
FPGA	Actel	A1280A-1CQ172B	7[1]	15**
FPGA	Actel	A14100A-2CQ256B	15[6]	26
128kx8 EPROM	SEI	27C010TRP-150	7[1]	15**
8M EEPROM	SEI	79C0832RP	30	52
4M SRAM	SEI	33C408RPF225Y-25	30	52
FIFO 16Kx9	SEI	7206ERPF225B	60[1]	103
Octal Buffer	Nat'l	RM54ACT244SSA	100[3]	172
Octal Bus TXCVR	Nat'l	RM54AC245SSA	100[3]	172
Quad RS422DR	Nat'l	DS26C32AMW/883	5[6]	11**
Quad RS422RX	Nat'l	DS26C31MW/883	5[6]	11**

Data: 1 = Sei, 2 = Harris, 3 = National Semi., 4 = SAIC, 5 = NASA, 6 = Boeing

* = Done for the LEO ONE orbit (950km x 950km 50 Degrees) with Rad Pak 1 Mission life, years calculated

** = RAD-PAK2

b) Single Event Effects (SEE)

SEE (Single Event Effects) forms possibly the most challenging design effort for the COTS single board computer designer.

i) Single Event Latch-up (SEL)

For SEL (Single Event Latch-up), device testing and screening are employed to prevent latch-up in most devices in the SB486R computer, and to predict the frequency of latch-up in susceptible devices. Generally, a latch-up threshold of 80MeV/-cm²/mg is considered latch-up free [3]. As seen in Figure F, all devices selected for the SB486R exhibit a threshold higher than 80MeV/-cm²/mg with the exception of the 486DX2 CPU, which exhibits a threshold higher than 60MeV/-cm²/mg . Although this results in infrequent latch-up

events, due to the CPU device threshold some protection must be provided. This is accomplished in three steps:

- If the watchdog timer times out, it is assumed that an SEU has occurred, and the CPU is reset.
- If the reset is successful, it is assumed the SEU is cleared and operation continues.
- If the reset is not successful, it is assumed a latch has occurred, and the SEi LPT™ device is triggered, crow-barring the CPU.

ii) Single Event Upset (SEU)

For Single Event Upsets, although SEU occurs rarely (see Figure 3 for SEE data), some improvement needs to be applied, as follows:

- For the CPU, the watchdog timer, augmented if needed with enlarged algorithms, detects improper operation typical of an SEU. This results in CPU reset.
- For memory, the SRAM (and DRAM if implemented) are continuously 'scrubbed' in background. The scrubbing rate and any resulting overhead are related to SEU requirements and are established for each mission. Since the EPROM and EEPROM will not see hard errors as a result of SEE, no protection is needed.
- I/O protection is related to the SEU resistance of the devices chosen. The SEU immunity of chosen devices ranges from good (available FPGAs) to excellent (selected ASIC technology).

SEE figures of merit are of course scenario-dependent. The data presented in Figure F are for a representative LEO orbit, [4]; a scenario-specific figure of merit may be developed as desired. In summary, both single event latch-up and upset are predicted only about 1E-4 days or so.

Table 3.: SEE Chart

Qty	Description	Source	SEL th	SEU th
1	CPU, 80486DX2	SEI	>40	<5.4
1	Prog. Counter	Harris	>80	none
1	Interrupt Controller	SEI	>80	11.4
2	Hex Schmitt Inverter	National	>120	none
2	Crystal Osc.	Q-Tech		
1	FPGA, Unprogrammed	Actel	>100	26*
2	FPGA, Unprogrammed	Actel	>112	15*
1	128kx8 OTP EPROM	SEI	>80	>80
1	8M (8x128Kx8) EEPROM	SEI	>120	120
8	4M (512Kx8) SRAM	SEI	>117	3
2	FIFO, Parallel, 16Kx9	SEI	>100	4
11	Octal Buffer	National	>120	none
9	Octal Bus Transceiver	National	>120	none
3	Quad RS422 Line Driver	National	none	none
2	Quad RS422 Line Receiver	National	none	none

* = C-C logic only

b) Techniques for SEU Improvement

SEi is working on strategies to improve SEE rates by a decimal or so; these will be discussed at the conference. Also of potential interest to the community are other SEi efforts dealing with development of a processor (SMX) which uses the ESA chip set, and a modular architecture for all single board computers allowing graceful selection of CPU, memory and I/O options.

D. Conclusion

A COTS strategy may be successfully implemented for both boost and payload space applications. Careful parts selection and use of the Rad-Pak® shielding package provide acceptable total dose hardness. Single Event Latchup (SEL) is mitigated by a combination of device selection and detection of critical non-operations with reboot or crowbar. Single Event Upset (SEU) will occur possible at an acceptable rate for boost missions. For payload mission, mitigation strategies in both hardware and software will reduce unconnected errors to acceptable values.