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Total Dose Hardness of a Commercial SiGe BiCMOS Technology

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Abstract

Over the past decade SiGe HBT technology has progressed from the laboratory to actual commercial applications. When integrated into a BiMOS process, this technology has applications in low-cost space systems. In this paper, we report results of total dose testing of a SiGe/CMOS process accessible through a commercial foundry.

I. Introduction

Over the past decade the requirements for increased high-frequency performance have pushed silicon-germanium heterojunction bipolar transistor (SiGe HBT) technology from the laboratory to a mature production process that is accessible through several foundries. A major advantage of the evolved SiGe technology is its compatibility with standard silicon wafer processing, which has enabled its integration into CMOS processes; this has led to important enhancements to the level of integration with respect to bipolar-only or MESFET-only processes.

The superior high-frequency performance of the SiGe HBT combined with high levels of integration make this an interesting technology for space applications, in particular for low earth orbit (LEO) commercial satellites. Here, the emphasis is on low cost and robust performance in a moderate radiation environment, with the very high levels of integration required by complex bandwidth on demand (BOD) systems. Representative SiGe device applications are in RF front end signal processing and in phased array antennas.

In this paper we report results of total dose testing of a commercially available SiGe HBT/CMOS foundry process. Total dose testing on preproduction SiGe devices has been reported earlier[1, 2]; here, we concentrate on the overall hardness of the as-supported foundry process in practical, moderate environments.

II. SiGe Process

HBT devices using epitaxial SiGe bases have been the subject of considerable R&D[3, 4, 5], and HBT-only processes have been available on a limited production basis. Higher levels of integration have resulted in requirements for more flexible processes, and the IBM SiGeHP process explored in this paper provides a practical solution. This process starts from the premise that a SiGe capability must be fully compatible with commercial CMOS production technology in order to be relevant to current requirements. The process enables integration of fast analog/RF signal processing with high performance logic, memory, digital signal processing (DSP) and embedded cores. The integration of high-frequency RF Signal processing reduces the need for single-device technologies such as the GaAs MESFET.

Compatibility with production CMOS is achieved through the use of CVD epitaxial base technology, in which the SiGe base region is grown over the collector region using a controlled relative Si:Ge concentration gradient. The HBT uses a polysilicon emitter that overlays the epi base region. This structure is compatible with the base half-micron CMOS process. The key application for the process are in RF signal processing, and the device list supports this objective; in Table 1, below, we show a partial list. The process uses n^- over p^- epitaxial starting material with deep trench isolation.

Table 1: Partial Device Listing

- Half-micron N- and P-channel MOS devices, with L_{eff} = .4 microns
- Epi base SiGe NPN HBT device, F_T > 60 GHz
- High speed Si lateral PNP device
- Silicon/insulator/silicon capacitors
- Metal/insulator/metal capacitors
- Spiral inductors
- Abrupt-junction tuning capacitors
- Up to five layers of interconnect metal
- Various resistors; fuses

The technology uses 3.3 volt supplies for the CMOS devices and up to 5 volts for the bipolars. It is characterized and modeled over the standard -55° to +125°C temperature range and is fully qualified on 8" wafers. The process is currently used at Harris Semiconductor for the production of RF front end parts for the Prism98™ spread-spectrum radio chip set, intended for commercial wireless LAN applications in the 2.4 GHz ISM band.

III. Radiation Effects

Historically, hardening of commercial BiMOS processes has been difficult, with a tradeoff between BJT performance (high implant activation temperatures) and MOS device hardness (limits on gate oxidation temperature). As feature sizes have decreased, basic MOS device hardness has improved due to reduced gate oxide volume available for charge trapping; this has combined with shallower, more heavily doped bipolar and generally cleaner oxides to improve overall hardness. Enhanced low dose rate response (ELDRS) remains a problem in most commercial technologies.

Previous work has reported [1, 2] excellent total dose hardness for the SiGe HBT. The high doping levels and thin emitter-base spacer dielectric both contribute to this hardness. Additionally, the use of an epi base process eliminates the oxide damage found in conventional BJT devices, as caused by high energy ion implantation[6]. Note also that these undamaged oxides are promising as a means of avoiding the ELDRS effects found in the nonhardened Si BJT device.

A second key issue is the hardness of the CMOS devices. Use of a thin gate oxide and of deep trench isolation are expected to yield good total dose immunity for these devices, with N-channel source-drain leakage a possible issue. In the balance of this summary we will describe testing methodology and initial results of radiation testing of both the SiGe HBT and CMOS devices. Complete results and conclusions will be presented in the final paper. Emphasis will be on the moderate total dose environment encountered in commercial space systems.

IV. Experimental Approach

We currently have testing in progress of both the SiGe HBT and CMOS devices of the IBM SiGeHP process, using samples drawn from foundry production wafers. Test devices were taken from several wafers and were packaged in standard hermetic dual-in-line packages; note we have chosen to avoid the added variables introduced by plastic packaging for the time being, in an effort to focus on the basic technology.

A. The HBT device.

As the HBT is a standard production device, the Si:Ge proportion in the epi base is fixed, and no permutations are being tested or are indeed even available. Irradiation was done using a Gammacell-220™ ^{60}Co source, at a dose rate of 130 rad(Si)/sec; this is a fast 'qualification' dose rate, with the lower dose rates of interest for enhanced low-dose rate response (ELDRS) running well below 1 rad(Si)/s. Plans for a subsequent low dose rate experiment are presently being developed. Several device geometries are available on each test die. Irradiation bias consisted of grounding all device terminals; this is not a worst-case configuration but is representative of actual low-voltage RF applications. Not that particular care in fixture construction is required here in order to avoid oscillation effects. Device characterization consisted of Gummel plots of I_c and I_b vs. V_{be}, gain vs. collector current (β vs. IC) plots and low-voltage device leakage measurements. We have currently completed 300 Krad(Si) total dose irradiation with excellent results; the HBT devices displayed negligible parameter shifts at this level.

B. CMOS Devices.

For these devices we use the same ^{60}Co irradiation facility, with suitable fixturing biasing the gate electrode of each device positive and grounding all other terminals. Using the same levels, these devices will be tested for subthreshold characteristics using I_d vs. V_{gs} plots and transcon-ductance using g_m vs. $|V_{gs}-V_t|$ plots. Testing of n-channel devices is currently under way.

V. Conclusion

High-performance SiGe HBT/CMOS processes are promising for low-cost commercial satellites with heavy dependence on RF signal processing and DSP. The IBM SiGeHP process provides a powerful, accessible capability at competitive cost. In this paper we report SiGe and CMOS device hardness at moderate total dose levels representative of LEO environments.

References

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