EVALUATION OF ACCELERATED TESTS PARAMETERS FOR CMOS IC TOTAL DOSE HARDNESS PREDICTION

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Abstract

The approach to accelerated test parameters evaluation is presented in order to predict CMOS IC total dose behavior in variable dose-rate environment.

The technique is based on the analytical model of MOSFET parameters total dose degradation. The simple way to estimate model parameter is proposed using IC's input-output MOSFET radiation test results.

I. INTRODUCTION

Nowadays total dose test procedure for IC is specified by MIL-STD883 - 1019.5 method. The procedure is excessively conservative respecting to the low-dose-rate environment that may lead to hardness underestimation and thus may be crucial for commercial IC's. Besides, the unified accelerated test conditions (annealing temperature and duration) don't guarantee the complete relaxation of radiation-induced charge within the specified time period, especially taking into consideration the latent processes [1].

The well-known less conservative cycled multi-step "irradiation-annealing" technique is based on irradiation and annealing alternate steps in order to simulate gradual dose absorption in low dose-rate range.

The purpose of this work is to develop the motivated procedure of cycled "irradiation-annealing" accelerated test parameters evaluation for CMOS IC total dose hardness prediction. The possible variable dose-rate time dependence (for example due to extreme space radiation flashes) as well as real process temperature and the probable contribution of latent relaxation processes should be taken into account.

II. METHOD DESCRIPTION

According to the model developed in [2] one can conclude that in order to simulate CMOS IC's behavior under irradiation with time-dependent dose rate $P_2(t)$ and at the temperature $T_2(t)$ the following condition should be realized in acceleration irradiation-annealing experiment.

The annealing process at step i is to be discontinued at the moment t_{ai} when n-channel MOSFET threshold voltage shift under laboratory irradiation is equal to the threshold voltage shift of the same device irradiated to the same total dose but with a lower dose rate P_2.

The moment t_{ai} can be obtained from the approximate equation:

$$\int_0^{t_{ai}} P_1(\tau)\ln\left[\frac{1}{t_0}\int_\tau^{t_{ai}}\exp\left(-\frac{W}{kT_1(\xi)}\right)d\xi\right]d\tau \approx \int_0^{t_{2i}} P_2(\tau)\ln\left[\frac{1}{t_0}\int_\tau^{t_{2i}}\exp\left(-\frac{W}{kT_2(\xi)}\right)d\xi\right]d\tau, \quad (1)$$

where $P_1(t)$ and $T_1(t)$ are dose rate and temperature during the test procedure, t_0 is time unit (1 s), W is the activation energy of oxide charge relaxation, k is Boltzman's factor. According to the model [3], the condition of the equality of interface trap densities can be described by the same equation with the different value of activation energy W.

The mentioned approximate equation (1) for the accelerated test conditions evaluation has the only one unknown parameter – activation energy W, which can be verified experimentally for any CMOS IC type without usage of special test structures (sect. III).

To simulate CMOS IC radiation behavior one must also take into account the latent processes [1]. Basing on the process mathematical model we suggest (in analogy with (1)) to determine the moment t_{ai} of annealing step i termination from the correspondence of interface trap densities, generated under low-dose and accelerated test irradiation:

$$\int_0^{t_{ai}} P_1(t_{ai}-\tau)\Psi(\tau,T_1)\,d\tau = \int_0^{t_i} P_2(t_i-\tau)\Psi(\tau,T_2)\,d\tau,$$

$$\Psi(t,T) = \frac{4}{\pi}\sum_{n=1}^{\infty}\frac{(-1)^{n+1}}{2n-1}\left(1-\exp\left(-\frac{\pi^2}{4}(2n-1)^2\frac{t}{t_D(T)}\right)\right)$$

$$t_D(T) = \frac{d^2}{D_H(T)}. \quad (2)$$

where d is IC's substrate width and D_H is the molecular hydrogen diffusion coefficient (in Si).

The irradiation dose at every step of accelerated test can be determined also from the model of MOSFET parameters radiation-induced degradation. The parasitic structures birds-beak leakage influence on IC's radiation tolerance is discussed in the full-size paper. The approach of the experimental estimation of the influence of the concurrent processes with different activation energies via accelerated test is suggested. The approach can be extended to take into account the dose-rate dependence of p-MOSFET parameters degradation.

The proposed acceleration test procedure was verified in experiment.

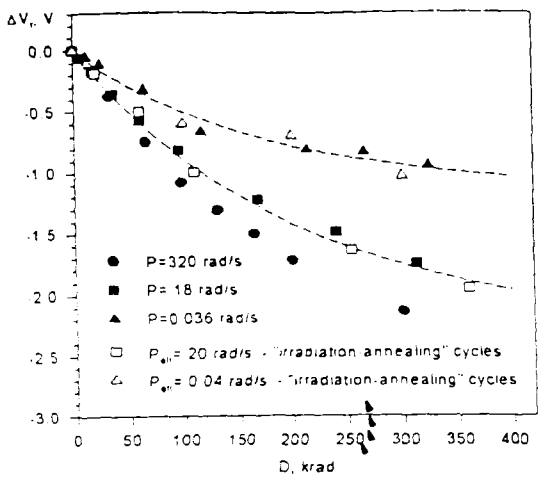

Fig. 1. The experimental comparative data of the "radiation-annealing" accelerated test and low-dose rate irradiation-induced n-MOSFET threshold voltage shift

Experimental results of the accelerated test with the determined parameters were in good agreement with the direct low- and medium-dose-rate irradiation data (fig.1).

III. Model Parameters Extraction

According to (1), the accelerated test conditions depends on the oxide charge relaxation and interface traps build-up activation energies. In practice, one can describe both processes via the single "effective" activation energy W with satisfactory tolerance. This parameter can be determined experimentally from the IC's n-MOSFET threshold voltage relaxation kinetics. In most of practical cases the specialized test structures for drain-gate characteristics measurements are poorly available. Therefore we suggest to extract the n-MOSFET threshold voltage from the IC's output device source-drain dependencies family, measured under several supply biases (fig.2).

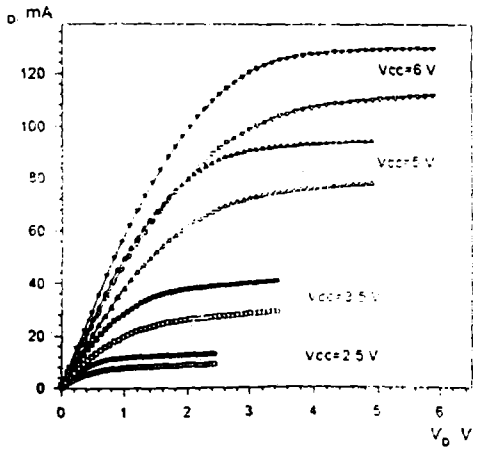

Fig. 2. The example of 1617RU6 SRAM output n-MOSFET source-drain dependencies total dose degradation, measured at various power supply voltages V_{cc}. Closed figures - pre-irradiated, open figures - post-irradiated dependencies.

It should be noted that the so-way determined activation energy of the relaxation processes is practically independent on the particular MOSFET on-chip geometry.

IV. Conclusion

The approach to cycled "radiation-annealing" accelerated test procedure parameters evaluation is developed, ensuring the simulation and prediction of CMOS IC's radiation behavior in variable dose-rate environment.

The technique presented is based on the analytical model dealt with the formation and thermally-activated tunnel relaxation of positive charge and interface traps buildup. The model single parameter - effective activation energy - can be determined experimentally from IC's on-chip MOSFET total dose test results without usage of specialized test structures.

The procedure makes it possible to consider extreme dose-rate flashes and to take into account the IC's parameters degradation due to latent relaxation processes as well.

The developed accelerated test technique is verified in comparative experiment in low-dose rate environment.

References

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