

## COMPARISON BETWEEN GROUND TESTS AND FLIGHT DATA FOR TWO STATIC 32 KB MEMORIES

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### Abstract

*The Microelectronics and Photonics Testbed (MPTB) carrying twenty-four experiments on-board a scientific satellite is in a high radiation orbit since November 1997. This paper presents SEU flight results on two commercial static RAMs included in two of the MPTB experiments.*

### I - INTRODUCTION

This paper presents flight data from the Microelectronics and Photonics Testbed (MPTB) project<sup>1</sup>. The study concerns two 32 K byte static memories, one from Hitachi (HM62256) the other (HM65756) from Matra MHS. The choice of these parts was motivated by the availability of ground test data [1-2,5] and flight data [3][6] for parts of the same date code. These circuits are presently in space aboard two different experiments included in MPTB [4]. The goal of these experiments is twofold: (a) obtain evidences about the fault tolerance properties of image processing approaches based on neural network algorithms and implemented by digital architectures, (b) get flight data on circuits previously evaluated in other space projects. This paper describes preliminary considerations concerning the second goal, derived from the analysis of data sent by these MPTB "neural boards".

MPTB was successfully launched in November 1997, flight data is available since 25th November. The actual environment is measured aboard MPTB using a particle telescope.

### II - EXPERIMENT DESCRIPTION

The architecture of the MPTB experiment referred B7 daughter board in the following, is depicted in Fig. 1.

Principal components of the boards are:

- the transputer T225: a reduced instruction set microprocessor (RISC) with parallelism capabilities. The T225 is the main core of the board, having in charge all the operations related with data transfer to/from the satellite and the implementation of DUT test strategies.
- a 4 Kbyte PROM (HM 6617) containing the object code of all the processes related with the operation of the board (boot, telemetry, telecommand, test programs and expected results).
- a 32 K byte SRAM (MHS HM65756) used mainly for the storage of T225 process workspaces and data. Also, the last 2Kbytes are reserved for telemetry and telecommand purpose. Then, about two thirds of its contents is observed by the transputer for upset detection and location.
- a 32 Kbyte SRAM (Hitachi HM62256) permanently screened by the transputer for the identification and location of upsets.
- a circuit for the detection of abnormal power consumption (latchup) and the corresponding recovering mechanisms.
- a watch-dog circuit, refreshed every 1.5 sec by the T225 in order to avoid system crashes due to SEU on T225 internal registers or flip-flops or on process workspaces.

In fact, this experiment is quasi identical to MPTB daughter board A7 excepted the absence of a dedicated neural co-processor (the L-Neuro from Philips Labs). Owing to the memory occupation constraints, two different detection methods were implemented: the first one is a classical memory test (RST: RAM Static Test) where a pattern stored in the DUT is periodically compared to expected results. The second one (CRC: Cyclic Redundancy Checksum) compares a signature associated with blocks of data (here 1Kbyte) being thus unable to identify the address of the bit modified as a consequence of a SEU. Fig. 2 illustrates the memory area occupation.

<sup>1</sup> MPTB project was designed by Naval Research Labs (NRL, Washington DC) aiming at providing flight data on novel microelectronics and photonics circuits off the shelf (COTS).

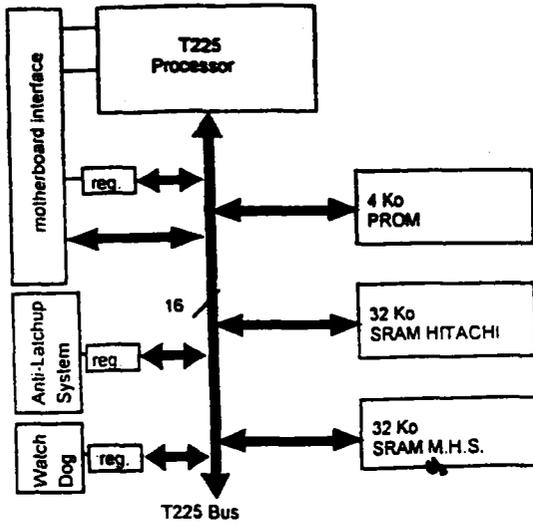


Fig.1: Block diagram of the MPTB-B7 board

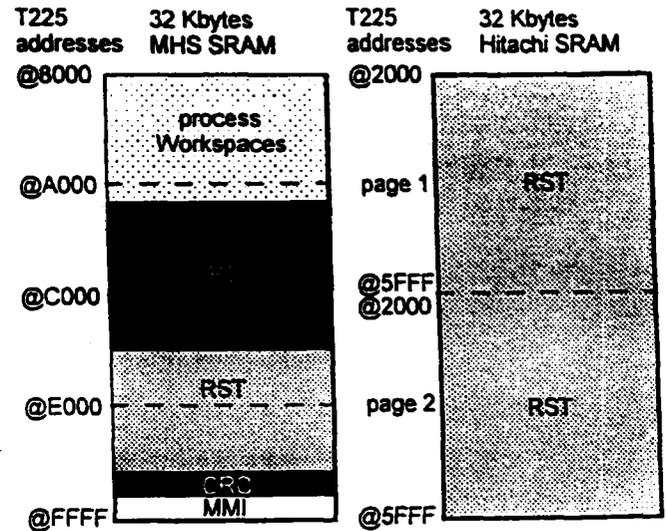


Figure 2: B-7 daughter board memory space organisation

### III - FLIGHT DATA ANALYSIS

The orbit of the spacecraft including MPTB experiments is highly elliptical, dipping below the earth's radiation belts and going all the way out to geosynchronous orbit. Therefore, during one orbit, the parts are exposed to an intense flux of protons and electrons in the radiation belts, where both SEE and total dose effects occur, as well as to the relatively low flux of highly energetic cosmic rays at apogee where the primary effects are SEE.

Flight data on memory SEU test sent by A7 and B7 neural boards after 12 months operation in space is summarised in Table 1. The results correspond to around one year (from end December 1997 to February 1999). For each detected SEU, the telemeter file precise the date and the flight time (generated by the motherboard) as well as the T225 process allowing its detection.

	HM62256	HM65756
#SEU	119	149
Error rate (seu/bit/day)	1.45 E-5	7.25 E-5
# Double Bit Upsets	5	2
Stuck-at-bit	yes	no

Table 1: Summarised results for one year flight

A total of 268 upsets were detected for the analysed period of time, 119 of them arising on the fully tested Hitachi SRAM, the remaining 149 occurring in different areas of the MHS SRAM.

As a preliminary conclusion it can be stated that the MHS SRAM is probably at least 4 times more sensitive to SEU than the Hitachi SRAM. This fact is confirmed by ground data [1,2].

The MHS SRAM sensitivity to multiple errors on adjacent cells was previously observed on ground and by EXEQ experiment onboard the MIR station [3].

The Hitachi memory has also exhibited what we call "stuck-at" bit errors. This kind of event is identified when the same address and data bit is found in error (fixed read data) for several consecutive read cycles. Table 2 presents for each event, the date of first and last occurrence. This behaviour has already been observed on SRAM 1Mbits memories [7] from other manufacturers and on the Hitachi 1Mbits product HM628128 [8].

This phenomenon is assumed to be induced by charged deposited in the gate region, and especially in the gate oxide, that generates a sub-threshold leakage on a transistor that makes the cell stuck at the written state. That means that the stuck-at-bit errors are detected with the opposite pattern to the one that is applied to the device during exposure.

This phenomenon may be induced by the interaction of one particle (heavy ion) or the cumulated total dose. For example, for the HM628128 device, Co60 experiments have shown that stuck-at-bit events start to occur at a dose level of 12 krad(Si) [8]. The combination of total dose/heavy ion irradiation lowers the dose level of occurrence of such errors. Total dose and heavy ion test are scheduled on the HM62256 device from the same date code of the flight devices. The results will be presented in the final paper and discussed.

@ hex bit [0-15]	board memory	first occurrence #orbit, date (d/m/yr hr:min:sec)	last occurrence #orbit, date (d/m/yr hr:min:sec)
@ : 5106 bit : 05	A7 Hitachi	# 760 20/11/1998 20:39:14	#791 06/12/1998 10:14:06
@ : 5b26 bit : 07	A7 Hitachi	# 765 23/11/1998 07:39:14	#767 24/11/1998 10:28:30
@ : 330e bit : 03	B7 Hitachi	# 764 22/11/1998 20:09:34	#786 03/12/1998 21:27:52
@ : 333e bit : 06	B7 Hitachi	# 764 22/11/1998 19:40:35	#764 22/11/1998 22:41:48
@ : 36c6 bit : 07	B7 Hitachi	# 778 29/11/1998 20:07:23	#781 01/12/1998 10:52:14
@ : 3ae6 bit : 06	B7 Hitachi	# 760 20/11/1998 21:21:34	#791 06/12/1998 09:36:41
@ : 3aee bit : 02	B7 Hitachi	# 762 21/11/1998 19:48:46	#806 13/12/1998 21:09:17
@ : 5406 bit : 03	B7 Hitachi	# 760 20/11/1998 19:47:05	#816 18/12/1998 22:21:49

Table 2: Stuck-at-bit errors on the Hitachi memories.

#### IV- COMPARISON WITH PREDICTED RATES

Cross-section data used for rate predictions were obtained on parts from the same flight lot (date code) that the parts flown on MPTB. In the case of HM65756, the cross-section values used correspond to flight parts retrieved from the EXEQ experiment on-board the MIR station [3]. Contrary to 62256, a sensitivity dispersion was observed and that is why in the following tables we indicate min and max values for HM65756.

Proton environment and upset rates have been calculated using the SPACERAD™ software in the following conditions :

- trapped proton model : AP8 (year 1964)
- date of calculation : 1965 (=1998-3x11 years)
- magnetic field model : DGRF65

These conditions correspond to the recommended conditions for flux calculations, i.e. to shift all dates back in time to the dates when the AP8 and AP9 models were built.

Heavy ion environment and rates have been calculated using the SPACERAD6 and CREME softwares in the following conditions :

- best approximation for cosmic ray fluxes  $\cdot M^{-1}$
- year 1995
- magnetosphere quiet

Four reference geometries have been taken into account for simulating the MPTB plateau :

- solid sphere of thickness 0.5, 1, and 2 mm Al
- a wide box 1m x 0.5m x 0.1m shielded at its top and sides with 1 mm Al and at its bottom with 100 mm Al, and supposed to represent the lightly shielded MPTB assembly mounted on the bulk of the carrier satellite.

Rates have been calculated using the actual proton and heavy-ion cross-section curves that we had previously measured [1-3], i.e. raw experimental data not fitted by any Weibull or Bendel representation.

Table 3 summarises the various proton rates obtained for the four geometries and the two devices. It shows that the rate does not depend much on shielding thickness in the case of spherical geometries, and that the calculation in the box leads to a rate lower by about a factor of two, which is consistent with considering that nearly half of the space is heavily shielded by the satellite. Table 4 gives the predicted heavy ion rates for the 1 mm Al sphere and the box.

Confrontation of SEU rates derived from predictions to those measured in flight is given table 5. As a conclusion and prior to a thorough analysis taking into account the geographic position of the events which will allow to separate proton and heavy-ion contributions, we may state that :

- error rate is underestimated for 62256 using standard prediction models
- error rate can be under or over estimated for 65756, but the dispersion on heavy-ion ground results does not allow to conclude

Device	Sphere 0.5 mm Al	Sphere 1 mm Al	Sphere 2 mm Al	Wide box
62256	4.2e-6	4e-6	3.8e-6	2.4e-6
65756	1.43e-5	1.36e-5	1.28e-5	8.12e-6

Table 3. estimated proton upset rates (upset/bit/day)

Device	Sphere 1 mm Al	Wide box
62256	4e-6	2.4e-6
65756 (min/max)	7.7e-6 / 1.3e-4	4.6e-6 / 7.9e-5

Table 4 : estimated heavy ion upset rates (upset/bit/day)

In almost one case, an underestimation has been observed. Further analysis for the final paper, will take into account a better shielding description of the MPTB (even though it is not the dominant factor), and the geographical repartition of events.

Device	Total estimated rate	Measured flight rate
62256	4.8e-6 to 8e-6	1.45e-5
65756	min 1.3e-5 to 2e-5 max. 8.7e-5 to 1.4e-4	7.25e-5

Table 5 : estimated and measured rates (upset/bit/day)

## REFERENCES

- [1] S. Duzellier, D. Falguère, J. Bourneau, R. Ecoffet, "Heavy ion/proton test results on high integrated memories", 1993 IEEE Radiation Effects Data Workshop, Snowmass 1993.
- [2] R. Ecoffet, D. Falguère, S. Duzellier, "Heavy ion test results on memories", 1992 IEEE Radiation Effects Data Workshop, New Orleans, 1992.
- [3] D. Falguère, S. Duzellier, R. Ecoffet, "SEE In-Flight Measurement on the MIR Orbital Station", IEEE Trans. Nucl. Sci., NS-41, n° 6, p., 1994.
- [4] James C. Ritter, "Microelectronics and Photonics Test Bed, Guidance and Control", *Advances in the Astronautical Sciences*, Eds. Robert D. Culp & Stuart B. Wiens, Published for the American Astronautical Society by Univelt, Vol. 94, pp. 139-150, 1997
- [5] R. Velazco, Ph. Cheynet, J-D. Muller, R. Ecoffet, S. Buchner, "Artificial Neural Network Robustness for on-board satellite image processing: Results of upset simulations and ground tests", *IEEE Trans. on Nuclear Science*, Vol 44, pp 2337-2344.1997.
- [6] R. Harboe Sorensen, E.J. Daly, L. Adams, C.I. Underwood, R. Miller, "Observation and Prediction of SEU in Hitachi SRAMs in low altitude Polar Orbit", *NSREC Vol 40, n6*, p 1498, 1993.
- [7] T.R. Oldham, K.W. Bennett, J. Beaucour, T. Carrière, C. Poivey, P. Garnier, "Total dose failures in advanced electronics from single ions", *NSREC Vol 40, n6*, p 1820, 1993.
- [8] J.P. David, J.G. Loquet, S. Duzellier, "Heavy ion-induced latent stuck bits revealed by total dose irradiation in 1Mb SRAMs", submitted to the 1999 RADECS conference