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# Total Dose Induced Increase in Input Offset Voltage in JFET Input Operational Amplifiers*

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## Abstract

Four different types of commercial JFET input operational amplifiers were irradiated with ionizing radiation under a variety of test conditions. All experienced significant increases in input offset voltage (Vos). Microprobe measurement of the electrical characteristics of the de-coupled input JFETs demonstrates that the increase in Vos is a result of the mismatch of the degraded JFETs.

## Introduction

It has been demonstrated in several studies [1-4] that the most sensitive electrical parameter for JFET input operational amplifiers is the input offset voltage, Vos, when the circuits are irradiated *under bias* at low dose rate [1-5] or at elevated temperature [3-5]. In the first papers reporting this response [1, 2] it was postulated that the cause of the increase in Vos was the degradation of the lateral pnp current source transistors in the second stage of the operational amplifier. In a recent study by Flament, et al, [3] it was shown that the offset voltage is determined primarily by the first stage of the amplifier, and that the value of Vos is determined by the difference in the gate voltage of the two input JFETs at a constant drain current. Many *discrete* JFETs have been shown to be very resistant to total dose degradation, primarily because they are majority carrier devices and the conduction channel is subsurface. However, as pointed in reference 3, integrated circuit JFETs often have a parasitic MOSFET element in their structure that is very sensitive to total dose, especially at low dose rate or elevated temperature. Thus while most discrete JFETs would not be expected to show significant degradation below 1 Mrad ($SiO_2$), integrated circuit JFETs may show significant degradation of drain current and pinchoff voltage at a few 10s of krad($SiO_2$). Although a strong case was made for the degraded Vos mechanism in reference 3, the actual device data were based on test structures and discrete transistors, not the actual integrated circuit JFETs. In this paper we will show that the actual circuit input JFET pair electrical characteristics of degraded circuits can explain the degraded Vos.

## Experimental details

The JFET input operational amplifiers used for this study were purchased as commercial off-the-shelf parts from a distributor. Each of the four part types, OP15, PM156, OP42 and OP249, was from a single date code lot, and all were manufactured by Analog Devices (formerly PMI). The parts were purchased in hermetically sealed packages, eight pin dual-in-line for the single amplifiers and 14 pin dual-in-line for the dual amplifier (OP249). The parts were used for a study to validate hardness assurance tests that have been proposed to address enhanced low dose rate sensitivity, ELDRS, in bipolar linear circuits [4, 5]. The irradiation test procedures and test conditions have been described fully in reference 5. For this study parts that had been exposed at 10 mrad($SiO_2$)/s to a total dose of 70 krad($SiO_2$) were selected for detailed examination, along with samples that had not been irradiated. One unexposed and one exposed sample of each part type was selected. Each part was electrically tested to verify that Vos was still degraded on the exposed parts, i.e., no significant annealing had taken place since exposure. The Vos readings on the exposed parts were all within a few mV of the post irradiation readings, and the Vos on the unexposed parts were all < 1mV. The package lids were removed and a photomicrograph was taken of each die type. It was learned from the photomicrographs that the OP15 and PM156 dies are identical in layout, down to the same chip release dates. This explains the nearly identical radiation response shown in reference 5 for these two part types. The dielectric overcoat was removed to allow easy separation of metal lines to isolate the individual input JFETs. Each de-coupled JFET was measured for the standard drain and gate I-V characteristics using microprobes to make contact to the source, drain and gate.

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## Experimental Results

The gate characteristics were measured by monitoring the drain current, Id, vs. gate voltage, Vg, for several steps of source to drain voltage, Vds, from 0V to -5V. Vg was swept from 0V to 3V. The gate characteristics (at Vds = -5V) for the two input JFETs, J1 and J2, are shown in Figures 1-4 for the four parts types, OP42, Op249, OP15 and PM156, respectively. The two curves with solid circles and squares are for the unexposed circuit (U) and the two curves with solid triangles and diamonds are for the exposed circuit (X). Each of the I-V characteristics are shown on semilog plots to emphasize the subthreshold region and more clearly show the pinchoff voltage, Vpo. In Figure 1 the OP42 shows a large shift in Vpo of about 0.7V. The degradation of Vpo for the other exposed JFETs is much less. In all four cases, however, the two exposed JFETs show a separation of the curves, whereas the two unexposed curves are nearly identical. To better show the separation of the exposed JFET pairs, the I-V characteristics are shown as linear plots in Figures 5-8 with the scales expanded. The separation of gate voltages for J1 and J2 at a fixed drain current determines the value of Vos. Table 1 is a comparison of the post irradiation value of Vos and the separation of Vg(J1) and Vg(J2) for each of the part types showing the excellent correlation between post rad Vos and the difference in gate voltages.

Table 1. Comparison of post rad Vos and Vg(J1) -Vg(J2)

| Circuit type | post rad Vos (mV) | Vg(J1)-Vg(J2) (mV) |
|---|---|---|
| OP42 | 35 | 28 |
| OP249 | 15 | 10 |
| OP15 | 32 | 38 |
| PM156 | 33 | 40 |

## Conclusion

**In this study we have presented data that provide direct support for the conclusions drawn in reference 3 concerning the source of the total dose induced change in Vos in JFET input operational amplifiers. Microprobe electrical measurements on de-coupled input JFETs in actual irradiated JFET input operational amplifiers have demonstrated that the Vos can be explained by the difference in the gate** voltage of the input pair at a constant drain current. In the final paper we will show cross sections of the actual circuit JFETs to identify the parasitic MOSFET that causes the degradation of the JFET. We will also show the results of SPICE circuit simulations that show how the degraded JFET electrical characteristics give rise to the post irradiation Vos.

## Acknowledgements

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## References

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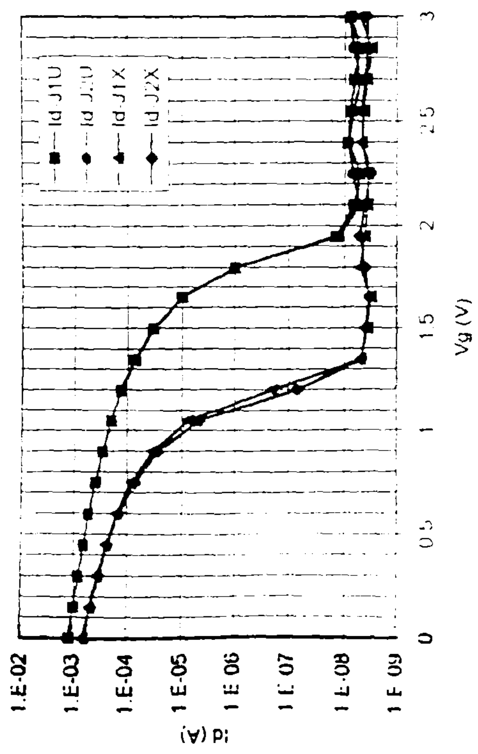


Figure 1. OP42 input JFET gate characteristics pre and post rad

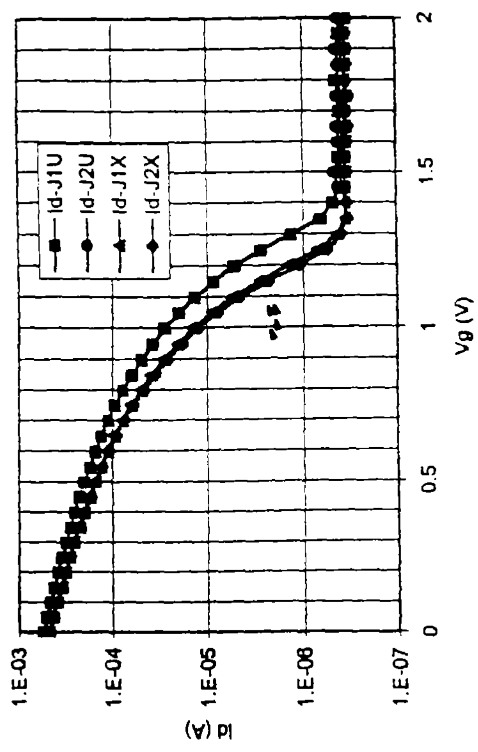


Figure 2. OP249, side 1, input JFET pre and post rad

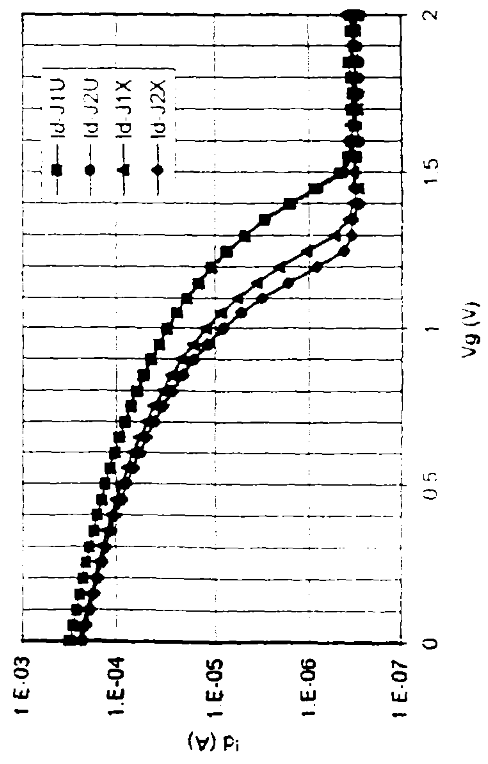


Figure 3. OP15 input JFET gate characteristics pre and post rad

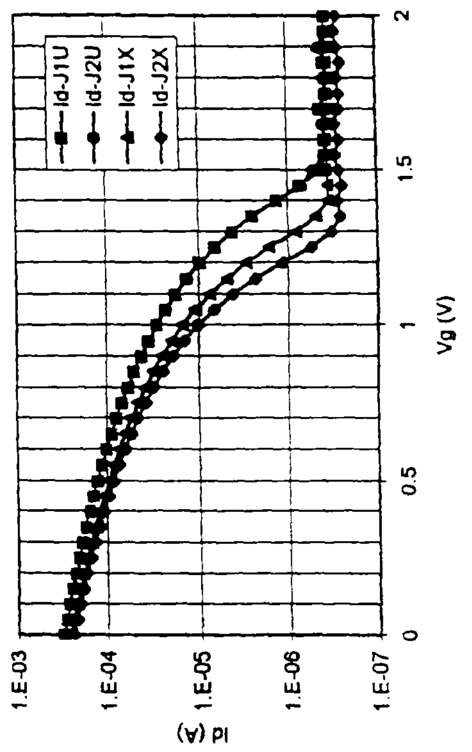


Figure 4. PM156 input JFET gate characteristics pre and post rad

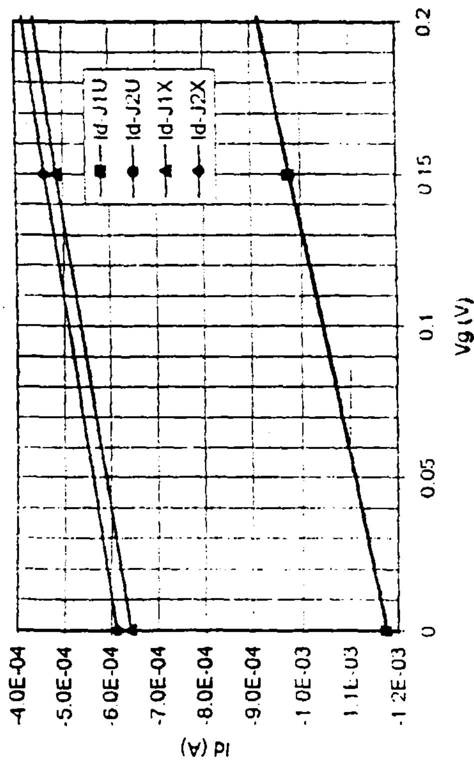


Figure 5 OP42 linear JFET characteristics pre and post rad

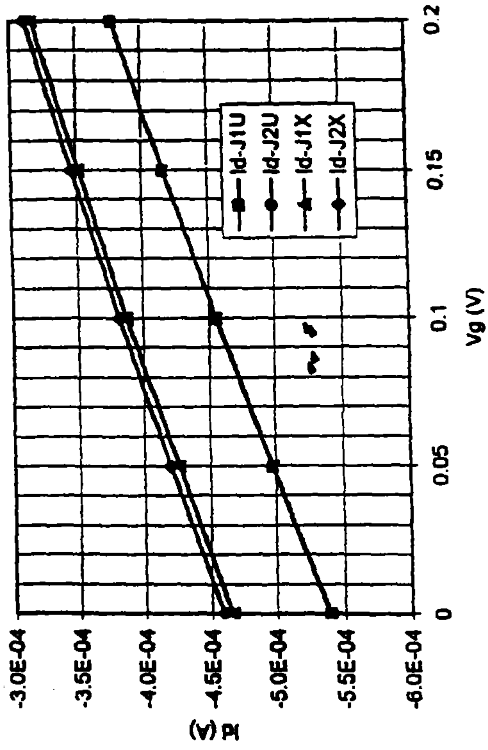


Figure 6. OP249 side 1 linear JFET characteristics pre and post rad

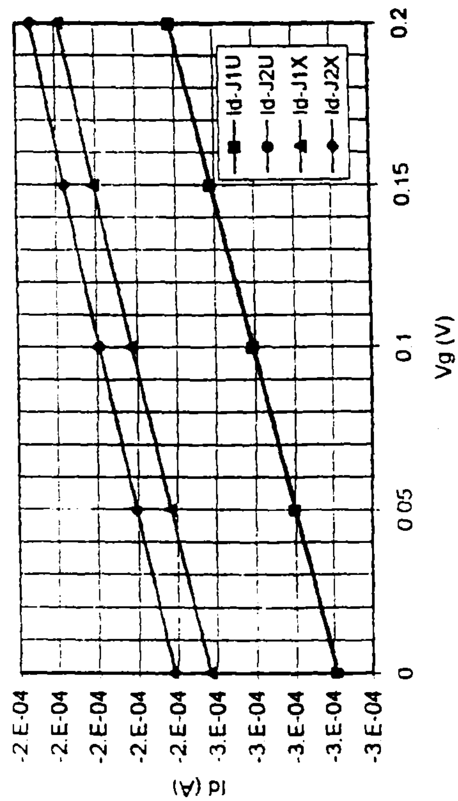


Figure 7 OP15 linear JFET characteristics pre and post rad

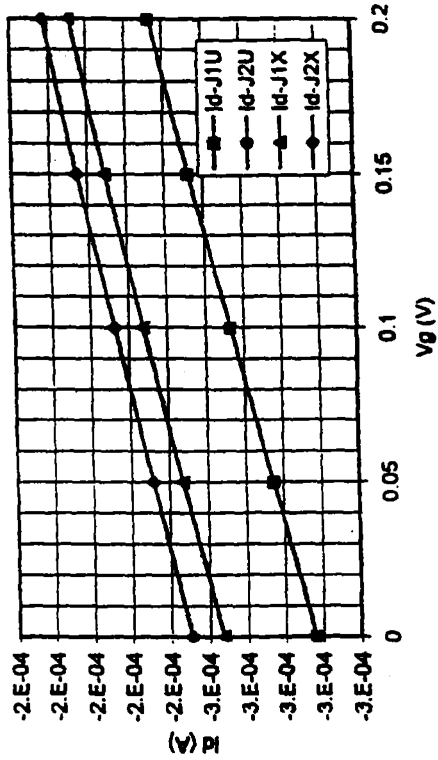


Figure 8. PM156 linear JFET characteristics pre and post rad