AN ANALYSIS OF RADIATION EFFECTS ON ELECTRONICS AND SOI-MOS DEVICES AS AN ALTERNATIVE

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ABSTRACT

The effects of radiation on semiconductors and electronic components are analyzed. The performance of such circuitry depends upon the reliability of electronic devices where electronic components will be unavoidably exposed to radiation. This exposure can be detrimental or even fatal to the expected function of the devices. Single event effects (SEE), in particular, which lead to sudden device or system failure and total dose effects can reduce the lifetime of electronic devices in such systems are discussed. Silicon-on-insulator (SOI) technology is introduced as an alternative for radiation-hardened devices. I-V Characteristics Curves for SOI-MOS devices subjected to a different total radiation doses are illustrated. In addition, properties of some semiconductor materials such as diamond, diamond-like carbon films, SiC, GaP, and AlGaN/GaN are compared with those of SOI devices. The recognition of the potential usefulness of SOI-MOS semiconductor materials for harsh environments is discussed. A summary of radiation effects, impacts and mitigation techniques is also presented.

Key words: Circuit Reliability, Electronic components, Radiation Damage, Radiation Effects, SOI

Introduction

There is a need to understand and combat potential radiation damage problems in semiconductor devices and circuits. Electronic systems in High Energy Physics experiments are exposed to radiation. Such hard environment provokes damages and errors in electronic devices. There are certain systems, such as space, in which radiation effects can be neglected. Reliability engineers should concern not only thermal, dynamical and atmospheric circumstances of space but also harsh radiations. In this review, radiation effects are introduced and discussed and alternative technologies are evaluated for different applications. The effects of radiation on semiconductor devices, radiation detectors, and electronic devices must be understood as well as high energy physics experiments which without a proper shielding may suffer severe failures. Emerging applications, detector technologies, circuit design techniques, new materials, and innovative system approaches are examined by many researchers [1].

The paper focuses on how a particular technology, namely Silicon On Insulator, is being used in the light of the above mentioned comments, rather than the mathematical foundations behind it. The present work

covers radiation-tolerant circuit implementations and MOS processing causing radiation damage. Radiation hardening of electronic devices is an extremely important field of such hard environments.
Generally speaking, semiconductor devices are housed in a ceramic "hardened" shell. This is primarily to prevent light from being absorbed at the junctions and changing the electric properties of the device. This is even more important if semiconductor devices are to be subjected to conditions harsher than the atmospheric conditions on the surface of the earth. For example, space is one of the harshest natural environments that devices are exposed to. In space, two types of radiation cause problems for semiconductor devices, namely the electromagnetic radiation (EM) and the ionizing radiation. EM radiation origin is mainly the Sun and consists of gamma rays photons, X-rays, ultraviolet or UV radiation, visible light, infrared, microwaves, and radio waves. Ionizing radiation may be made up of high-energy protons, helium nuclei, and heavy nuclei. These radiations are the most penetrating radiation because of their high energy. Depending on the total flux of these radiations they may or may not cause a problem for electronic devices. Thus, regions around electronic devices may comprise high-energy protons and electrons. Each type of radiation described has an individual effect on electronic devices and it is necessary to know which type of device will be exposed to know before against what is to be protected. Presented work undertakes only the most important points, because the problem is complex and very wide, exceeding the framework of this paper. The main purpose of electronic devices testing for radiation effects is to ascertain their compliance with certain regulations and standards, where some effects of radiation that might take place are Total Ionizing Dose Effects, Transient Dose Effects, and Single Event Effects, as will be described [1-3].

Radiation Sources and Mechanism

Radiation causes damages in electronic components, the type and magnitude of these damages depending on the irradiation environment. There are three main groups of mechanisms that illustrate radiation effects in semiconductor materials where high-energy particle or photon loses its kinetic energy in different mechanisms, thus creating various damages. These are, as follows [4]: *Displacement damage* (DD) due to Non Ionizing Energy Loss (NIEL), *Total Ionizing Dose* (TID) and *Single Event Effects* (SEE), respectively. DD is caused by neutrons, protons, alpha particles, heavy ions, and very high energy gamma photons. They change the arrangement of the atoms in the lattice. DD can be created by protons at all energies, electron with energies greater than 150 keV. Compared to TID and SEE, DD is less disturbing. Only a fraction of 1% of the energy loss goes into displacement process [5]. A typical DD effect would be gain degradation and leakage current in bipolar transistors. When neutrons strike a semiconductor chip, they displace atoms within the crystal lattice structure. The minority carrier lifetime is reduced because of the increased recombination centres created, [4].

Figure 1 represents an illustrative representation of collisions produced by X-Rays and other high energy radiation in an n-channel MOSFET thus generating electron-hole pairs in the gate oxide.

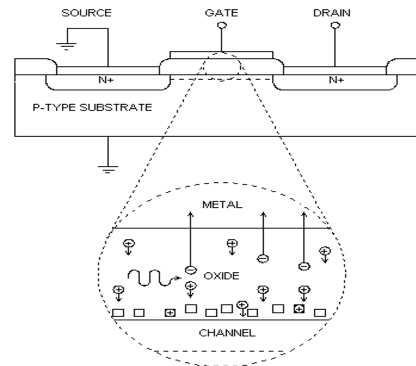

Figure 1 *Illustrative representation of collisions produced by X-Rays and other high energy radiation in an n-channel MOSFET generating electron-hole pairs in the gate oxide*

Whereas, particles associated with TID are categorized into three main groups relating to the source of the radiation: solar flare particles, cosmic rays, and trapped radiation belt particles, respectively. TID would cause energy deposition in silicon dioxide, because the electron-hole pairs created in this material do not completely recombine in a very short time. In the presence of an electric field in the oxide, a great amount of the pairs does not recombine, and both electrons and holes start to drift in the electric field. Electrons, with a much higher mobility, can easily leave the oxide. Holes instead can be trapped in defect centres in the oxide. Additionally, this process can produce or activate defects (interface states) at the silicon-silicon oxide (Si-SiO_2) interface. The charge build-up and the activation of defects are the two reasons for device degradation induced by TID. Charge build-up in the oxide is due to the trapping of holes in the oxide. This happens in the bulk of the oxide. For the gate oxide of MOS transistors, these charges will screen or enhance, depending on applied gate voltage, the gate electric field. This will lead to a threshold voltage shift. Interface states trap charge from the channel, which leads to both a threshold voltage shift and also affects the mobility of carriers in the channel. The two types of effects, namely the trapping of holes and the creation of interface states, have different dynamics. However, the effects can be shared in two categories. These are silicon inversion under a thick oxide, opening a conductive channel and effects decreasing the gain of the transistor [5].

For transistors, both n-p-n and p-n-p transistors show an enhanced degradation at low dose rate (when they show it) and their excess base current increases by a factor typically 10 to 20 more at low dose rates compared to high ones.

On the other hand, SEEs are very localized event induced by a single particle, whilst TID and DD are gradual cumulative effects. SEE is an instantaneous failure mechanism and expressed in terms of failure rate. SEE results from, as the term suggests, a single, energetic particle. SEE can lead to transient errors giving spurious signals propagating in the circuit. Transient errors are frequent in analogue circuits, or in combinational logic. They sometimes propagate to a latch and become static. Static errors lead to overwriting information stored by the circuit. Static errors can be corrected by outside control. Since they overwrite information stored in the circuit, a rewrite or power cycle can correct the error with no permanent damage. Permanent or hard errors are those leading to a permanent error, which can be the failure of the whole circuit (destructive). SEEs occur when a single high-energy particle strikes a device, leaving behind an ionized track. The ionization along the path of the impinging particle collects at a circuit node. If the charge is high enough, it can create a soft error, called Single Event Upset (SEU), such as a bit flip, a change in state that causes a momentary glitch in the device output, or corruption of the data in a storage element. A SEE can possibly trigger a device latchup and burnout. Latchup occurs when sufficient current is induced in part of the device that causes the device to latch into a fixed state

regardless of circuit input. Burnout occurs when the radiation induces sufficient power dissipation to cause catastrophic device failure. SEEs may be divided into the following effects (in order of permanency) [6-9]:

a) ***Single Event Upsets (SEU)*****:** These are also known as soft errors that occur due to either the deposition or depletion of charge by a single ion at a circuit node, causing a change of state in a memory cell. This type of event causes no permanent damage and the device can be reprogrammed for correct function after its occurrence.

b) ***Single Event Latchup (SEL)*****:** This effect can occur in any semiconductor device which has a parasitic n-p-n-p path. It can be soft or hard error. A single heavy ion or high energy proton passing through either the base emitter junction of the parasitic n-p-n transistor, or the emitter-base junction of the p-n-p transistor can initiate regenerative action.

c) ***Single Event Snapback*****:** This is also a regenerative current mechanism resembling SEL, but a device does not require a p-n-p structure. It can be triggered in a n-channel MOS transistor with large currents by a single event that may induce an avalanche multiplication near the drain junction of the transistor.
d) ***Single Event-Induced Burnout (SEBO)*****:** This is a hard failure occurring in power MOSFET, BJT and power diodes (see **Figure 2**). For example, this event may occur in power MOSFETs when the passage of a single heavy ion forward biases the thin body region under the source of the device.

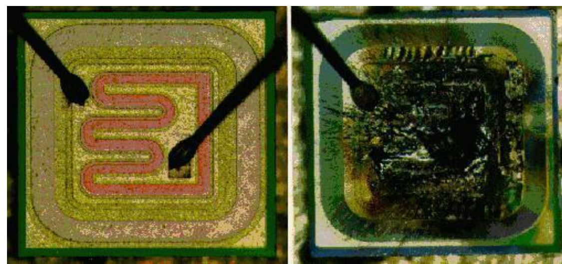

Figure 2 *Semiconductor before and after a Single Event-Induced Burnout [8]*

e) ***Single Event Gate Rupture (SEGR)*****:** This effect occurs when a single ionizing particle leads to a conducting path in a power MOSFET. This has been observed due to heavy ion hits in power MOSFETs when a large bias is applied to the gate, leading to thermal breakdown and destruction of the gate oxide (**Figure 3**) [9].

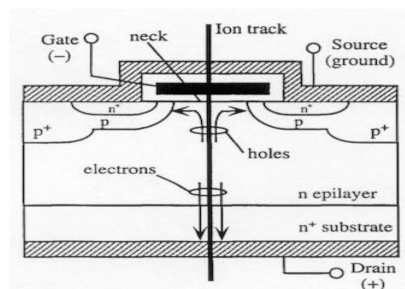

Figure 3 *SEGR caused by a heavy ion striking the middle of the gate oxide of a MOSFET*

SOI Devices as an alternative

While Silicon-on-insulator, SOI, has already become a mature technology for low power CMOS circuits and reasonably represents the main manufacturing technology for the next generation of ULSI low power circuits, it is still an emerging technology for high voltage power ICs. Compared to bulk junction isolated devices, SOI devices offer improved isolation, reduced leakage currents and faster switching speed. This technology offers the possibility of building electronic devices in a thin layer of silicon that is electrically isolated from the thick semiconductor substrate through the use of a buried insulating layer (**Figure 4**). In the standard silicon technology the semiconductor substrate is associated with undesirable effects such as high leakage currents, parasitic bipolar components, and, more importantly, interference between individual active devices.

The first confirmation that SOI technology is becoming the state-of the art technology in low-power ICs came in 1999, when IBM launched the first fully functional SOI mainstream microprocessor. Besides the fast speed, other benefits of the new SOI chip are reduced power consumption (up to 3 times) and a small soft error rate [10-12].

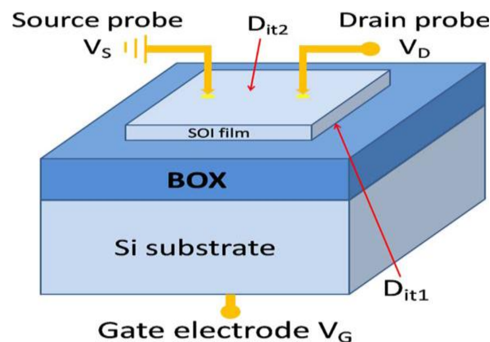

Figure 4 *A schematic diagram for the SOI MOSFET, where D_{it} is the interface traps*

In nanotechnology and microelectronics where low power consumption and high speed are desired, devices with nano and submicron dimensions are essential as well as devices that are radiation hardened. SOI technology is an attractive choice for these applications. SOI MOS devices have received great attention due to their advantages over conventional bulk MOSFETs [10] such as: lower parasitic capacitance, improved sub-threshold characteristics and reduced short-channel effects as well tolerance to radiation effects. So to gain insight into the physics of the device and evaluate their performance, an accurate model of the device parameters is essential. The threshold voltage (V_{th}) and Capacitance-Voltage (C-V) characteristics are important features for characterization of the performance of SOI MOSFETs [13]. However, these characteristics are dependent on a wide range of parameters such as: thickness of the channel, front and buried oxide thickness, channel and substrate doping, temperature etc. In ultrathin channel devices, the threshold voltage is influenced by operating temperature of the environment. The temperature dependence of V_{th} of accumulation-mode SOI devices has been reported in literature [14]. Moreover, we have shown previously that C-V characterization is well established mean for characterizing the strong inversion condition of SOI devices [15].

The buried oxide (BOX) inherent to an SOI transistor is the major difference in the total-dose response between bulk-silicon and SOI technologies. BOX has direct effects on leakage currents. Ionizing radiation induces the build-up of net positive charges in the buried oxide near the silicon-buried oxide interface and interface traps at the interface. The radiation-induced charge can reverse the bottom surface of the silicon channel forming a conducting channel (back channel) between the source and the drain of the transistor.

For fully-depleted transistors, the back-channel leakage is strongly affected by gate bias. The bias on the bottom substrate can strongly affect the radiation response. The radiation response of buried oxides has been found to be highly dependent on the fabrication process. SIMOX buried oxides are fabricated by implanting substrates with oxygen at high dose levels and energies. As such, it is natural to expect that the oxide may include numerous implant related defects throughout the buried oxide that can trap radiation generated charge. Up to 100% of the radiation generated holes are trapped in the bulk of the oxide at deep trap sites close to their point of origin.

Another harsh environment that can benefit from the hardness advantages of SOI circuits is that of high-energy particle accelerators. Devices also must be able to survive without upset or latchup the heavy particle jets and secondary cascades associated with the accelerators. The heavy particle jets and secondary cascades are similar to the cosmic ray heavy ions. SOI technology also provides these devices with good SEU immunity. In addition to being susceptible to soft errors due to cosmic rays in the space environment, advanced silicon ICs also will be susceptible to single-event upset on earth and in low altitude aircraft due to cosmic rays that penetrate the earth's atmosphere and due to energetic particles emitted from other sources. For example, alpha particles can have LETs high enough to cause SEU in commercial ICs. If the alpha particles are generated outside the IC substrate, they can be effectively attenuated using polyimide or other insulating coatings on the IC. These problems can be reduced or mitigated by using SOI technology. Cosmic rays at the earth's surface consist primarily of neutrons, protons, electrons, and muons. Those particles most important for SEU are protons and neutrons. Shielding of these particles is normally not practical. The LETs of both neutrons and protons are too small to directly cause SEU in present-day ICs. However, both neutrons and protons can generate secondary particles (e.g., alpha particles) by nuclear interactions with LETs high-enough to cause SEU [1].

Experimental Results and Discussion

The data used in this paper are for a 0.25 μm fully depleted (SIMOX) SOI CMOS device that was exposed to 62.5MeV protons and irradiated at the room temperature. During irradiation, the front-gate was biased at 2.0 V, and all of the other terminals were grounded. These devices were subjected to an equivalent total gamma doses ranging from of 600 Gy and 1500 Gy at room temperature [16].

Figure 5 shows drain current (I_D) as a function of the front-gate voltage (V_{GS}) for at different radiation doses. Increasing the dose, the leakage current increases somewhat. However, such an increase in conventional MOS devices may lead to non-ideal sub-threshold behaviour in the I_D-V_{GS} characteristics curve. This leakage current is attributed to the current of the lateral parasitic transistor where the observed shift in threshold voltage can cause the device to change the status of its operation region. This shift can be attributed to the presence of energetically localized donor-like electron trap states at the Si-SiO_2 interface.

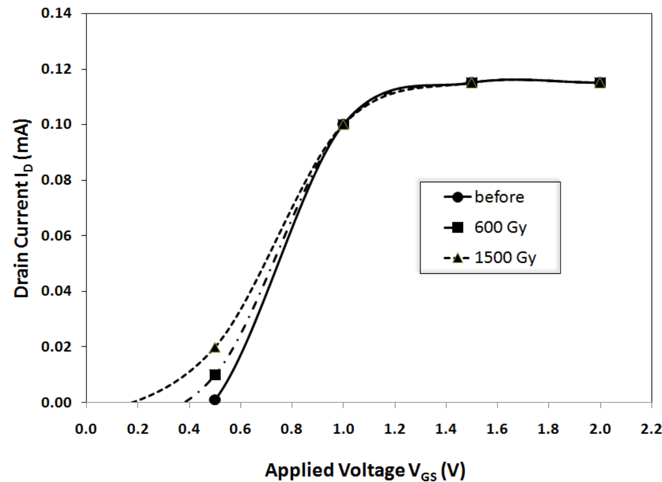

Figure 5 *I-V characteristics curves for a SIMOX SOI-MOSFET subjected to a different total radiation doses*

Non SOI Devices

Diamond and some diamond-like semiconductors are also very interesting. The unique combination of material properties of diamond, such as piezoresistivity, mechanical hardness, low coefficient of friction and high thermal conductivity makes it ideal for applications such as physical sensors and MEMS. The wide gap of diamond indicates that the piezoresistive effect is "hard", that means it is preserved at higher temperatures and in radiation environments that severely limit present materials. Silicon devices and most traditional integrated circuits made of Si are not able to operate at temperatures above 150 ^{o}C, especially when high operating temperatures are combined with high-frequency, high-power, and high-radiation environments. Considerable interest in recent years in WBG semiconductors and devices is especially connected with two important classes of applications, namely blue/green and white light emitting diodes and lasers as well as high-power, high frequency, high temperature electronics. As an example, for optoelectronics applications, GaP, AlGaN, GaN, and other diamond and diamond-like devices (WBG semiconductors) are leading materials because they are direct band-gap materials which give them a huge advantage over the indirect gap SiC, although it has been used for a long time for the manufacture of LEDs. Diamond and diamond-like carbon actually have very good parameters, but problems with producing large single crystals and doping delay their applications. GaN and AlGaN have the advantage of the availability of heterostructures and excellent transport properties, but they have poorer thermal conductivity in comparison with silicon carbide. Doping limits and band-gap engineering in WBG semiconductors, their epitaxial growth, solving of problems of manufacture of ohmic contacts to WBGs, plasma and dry etching and ion implantation are in the focus of attention of researchers. Much attention has been given to SiC, currently the most mature of the wide band-gap (2.0 eV $< E$g $<$ 7.0 eV) semiconductors, as a material well suited for high-temperature, high-frequency, high-radiation environments and efficient high-power operation (i.e. harsh environment) [17].

Overview of radiation mitigation techniques

To assure proper electronic devices operation there are several radiation mitigation techniques such as: conventional shielding, devices dedicated to work in irradiation environment and appropriate system design. These ideas and methods, presented in details in [1-2], are briefly discussed below. **Table 1** summarizes radiation effects, sources, impacts, mitigation techniques and time scale.

Table 1 *Overview of the radiation effects in semiconductor devices.*

Effect	*Source*	*Result*	*Mitigation*	*Time Scale*
TID	*dominated by protons, and electrons for planetary missions*	*threshold shifts, increased leakage and power consumption*	*Shielding (effective for electron)*	*Long*
DD	*neutrons, protons, alpha particles, heavy ions, and very high energy gamma photons*	*gain degradation and leakage current in bipolar FETs*	*(partly) shielding*	*medium/long*
SEE	*heavy ions, protons, neutrons*	*change state of memory, latch-up, damage to gate oxide*	*Redundancy, power cycling, latch-up protection circuit*	*instantaneous*

Conclusions

The radiation type and effects, depending on location and timing, are discussed. Proton radiation data on 0.25 μm fully depleted SOI MOSFETs fabricated on SIMOX wafers are presented. For the front-gate characteristics, the SOI devices do not show large sub-threshold currents. The buried oxide, inherent to SOI MOSFETs, reduces the effect of parasitic capacitances that are usually triggered in MOS devices.

The usefulness of the SOI technology is presented as an alternative for harsh environments where, despite exposure to significant radiation doses, the SOI devices remained functional before and after irradiation. These measurements ascertain that radiation induced defect generation mechanisms in the SOI devices need to be further considered both experimentally and theoretically.

The present data clearly indicate that SOI devices are satisfactorily radiation tolerant to be useful for harsh environment applications. Possible mitigation techniques, which are used to guard against the harmful effects where no single solution exists for all impacts, due to various radiation sources are presented.

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