ULTRA-LOW POWER THIN FILM TRANSISTORS WITH GATE OXIDE FORMED BY NITRIC ACID OXIDATION METHOD

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1. Abstract

We have developed a low temperature fabrication method of SiO_2/Si structure by use of nitric acid, i.e., nitric acid oxidation of Si (NAOS) method, and applied it to thin film transistors (TFT). A silicon dioxide (SiO_2) layer formed by the NAOS method at room temperature possesses 1.8 nm thickness, and its leakage current density is as low as that of thermally grown SiO_2 layer with the same thickness formed at ~900 ºC. The fabricated TFTs possess an ultra-thin NAOS SiO_2/CVD SiO_2 stack gate dielectric structure. The ultrathin NAOS SiO_2 layer effectively blocks a gate leakage current, and thus, the thickness of the gate oxide layer can be decreased from 80 to 20 nm. The thin gate oxide layer enables to decrease the operation voltage to 2 V (cf. the conventional operation voltage of TFTs with 80 nm gate oxide: 12 V) because of the low threshold voltages, i.e., –0.5 V for P-ch TFTs and 0.5 V for N-ch TFTs, and thus the consumed power decreases to 1/36 of that of the conventional TFTs. The drain current increases rapidly with the gate voltage, and the sub-threshold voltage is ~80 mV/dec. The low sub-threshold swing is attributable to the thin gate oxide thickness and low interface state density of the NAOS SiO_2 layer.

2. Introduction

Development of low temperature oxidation methods of Si is of importance not only from academic viewpoint but also for application to thin film transistors (TFTs). A thermal

oxidation method which can form high quality SiO_2/Si structure but requires high temperatures above 800 ºC cannot be used for fabrication of TFTs because of low softening temperature of glass substrates at ~500ºC. Conventional low temperature fabrication of SiO_2/Si structure employs deposition methods such as plasma-enhanced chemical vapour deposition (PECVD). Using the deposition methods, however, a uniform thickness SiO_2 layer cannot be formed especially on rough poly-crystalline Si (poly-Si) surfaces with ridge structure (cf. Fig. 1), resulting from laser annealing of amorphous Si thin films to crystallize [1]. A leakage current flows through thin regions, and to achieve a sufficiently low leakage current, a thick gate oxide layer is necessary. The interfacial characteristics of the SiO_2 layer formed by the deposition method are poor (e.g., high interface state density [2,3]) because of incomplete bond formation at the interface and presence of contaminants before deposition. Bulk characteristics are also poor because of incorporation of undesirable species such as water and hydrocarbon, and low atomic density of the SiO_2 layer [4,5]. Because of these disadvantages, a thick gate oxide layer of ~80 nm is required for TFTs. The thick gate oxide layer increases the operation voltage and power consumption because the consumed energy is approximately proportional to the square of the operation voltage. The thick gate oxide layer also makes shrinkage of TFTs difficult.

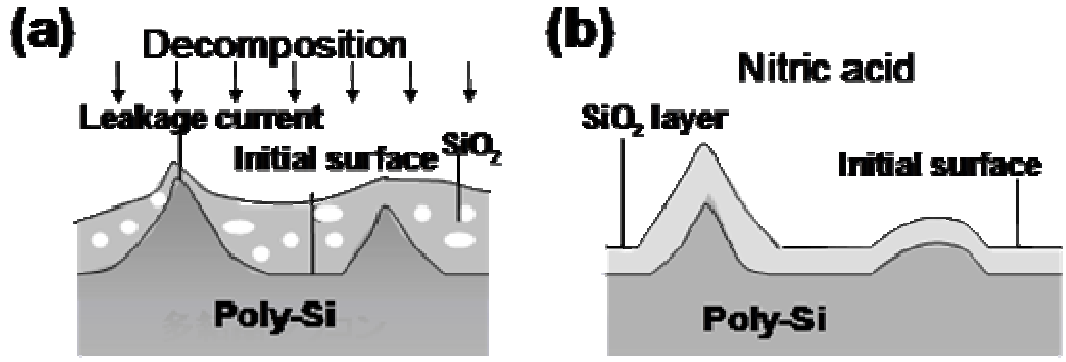

Fig.1: *Comparison of conventional deposition methods (a) such as PECVD and the NAOS method (b) for low temperature fabrication of SiO_2/Si structure.*

The disadvantages of the deposition methods can be avoided by direct oxidation methods at low temperatures such as plasma oxidation [6,7], metal-promoted oxidation [8,9], ozone oxidation [10], UV-enhanced oxidation [11], etc. However, these methods possess different disadvantages, e.g., plasma damage for plasma oxidation, and metal contamination for metal-promoted oxidation. We have developed a low temperature fabrication method of SiO_2/Si structure by use of high concentration (i.e., higher than that of azeotropic mixture of

HNO_3 with water of 68 wt%) nitric acid aqueous solutions [12-16]. The oxidation proceeds via reactions of oxygen atoms and/or dissociated oxygen ions (i.e., O^-) with Si. The activation energy for the interfacial reaction is low due to their high oxidizing activities, and that for the diffusion is also low due to their small sizes. Because the NAOS method is a direct oxidation method, a uniform thickness SiO_2 layer can be formed even on rough Si surfaces (cf. Fig. 1b). Because an SiO_2/Si interface is formed in Si bulk before oxidation, excellent interfacial characteristics can be achieved. It has been found that the bulk characteristics are also good because of higher atomic density than thermal oxide [13].

In the present study, this NAOS method has been applied to fabrication of gate oxide in TFTs by the formation of ultrathin NAOS SiO_2/~20 nm CVD SiO_2 stack gate dielectric structure. The TFTs can be operated at 2 V, and possess a high on/off ratio of 10^9 and low sub-threshold swing of ~80 mV/dec.

3. Experiments

A silicon nitride layer of ~100 nm thickness was deposited on glass substrates to prevent diffusion of contaminating species from the glass substrates. Then, amorphous Si thin films were deposited, followed by laser annealing to crystallize. The poly-Si layer thus produced possessed approximately 50 nm thickness. Then, an ultrathin SiO_2 layer was formed by immersion of the specimens in 68wt% HNO_3 aqueous solutions at room temperature, followed by deposition of ~20 nm thick SiO_2 layer by use of the PECVD method.

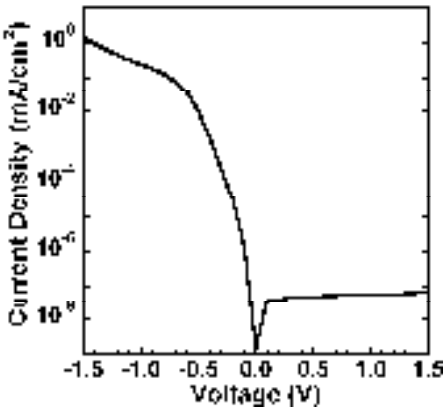

Fig. 2: *Leakage current density vs. the gate voltage for the 1.8 nm thick SiO_2 layer formed on Si(100) by use of the NAOS method at room temperature.*

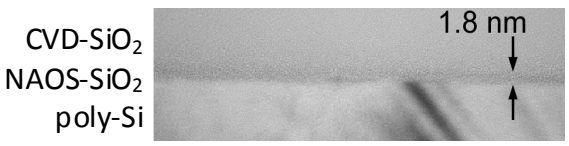

Fig. 3: *TEM micrographs of the TFTs with the ultra-thin NAOS SiO_2/CVD SiO_2 stack gate dielectric structure.*

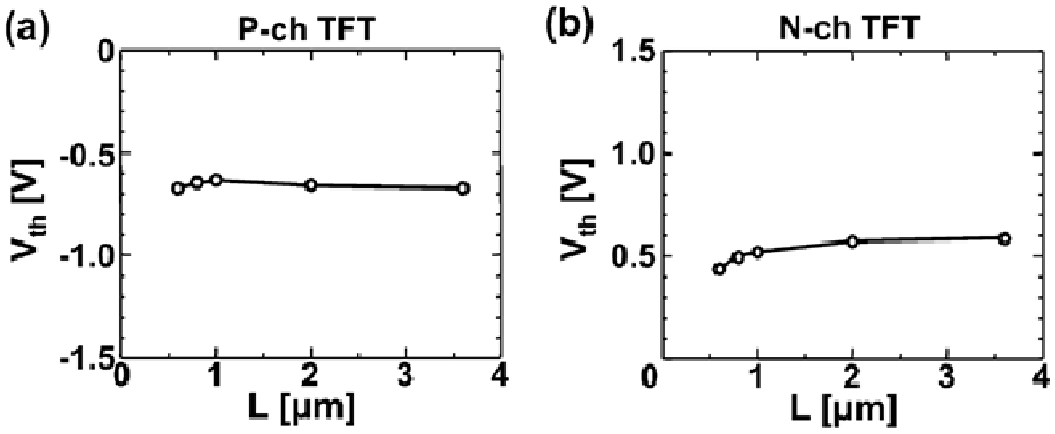

Fig. 4: *Threshold voltages of the P-ch (a) and N-ch (b) TFTs with the ultra-thin NAOS SiO_2/~20 nm CVD SiO_2 stack gate dielectric structure.*

Source and drain regions were defined by implantation, and gate electrodes were produced by deposition of a tungsten layer. X-ray photoelectron spectroscopy (XPS) measurements were performed using a VG Scientific ESCSLSB 220i-XL spectrometer with a monochromatic Al Kα radiation source. Photoelectrons were collected in the surface-normal direction.

Transmission electron microscopy (TEM) measurements of the TFT specimens were carried out using a JEOL EM-3000F with a 300 keV incident energy.

4. Results and discussion

Figure 2 shows the current-voltage curves of the ultrathin NAOS SiO_2 layer formed on single crystalline n-Si substrates with the (100) orientation. The inset shows the XPS spectra in the Si 2p region. From the ratio in the area intensity between the SiO_2 peak and the Si substrate peak, the SiO_2 thickness was estimated to be 1.8 nm.

The circle in the figure shows the leakage current density of a thermal oxide layer with 1.8 nm thickness [15]. It is clearly seen that the leakage current density of the NAOS SiO_2 layer was as low as that of a thermal oxide with the same thickness.

Figure 3 shows the cross-sectional TEM micrograph of the stack gate dielectric structure on poly-Si. The NAOS SiO_2 layer possessed a uniform thickness of 1.8 nm even in the presence of the grain boundary and thus on the two different oriented Si surface. The gate oxide layer possessed approximately 20 nm thickness. A NAOS SiO_2 layer was clearly observed at the SiO_2/Si interface with a colour darker than that of the CVD SiO_2 layer.

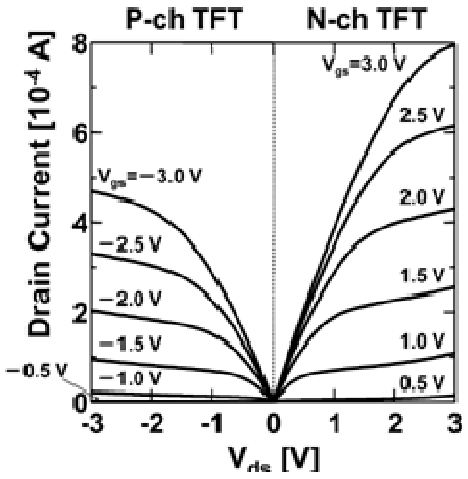

Fig. 5: *I_d-V_{s-d} curves for the P-ch and N-ch TFTs with the ultra-thin NAOS SiO_2/~*20 nm *CVD SiO_2 stack gate dielectric structure.*

The darker colour indicates a higher atomic density of the NAOS SiO_2 layer than that of the CVD SiO_2 layer. We found that the NAOS SiO_2 layer possesses an atomic density of 2.34×10^{22} atoms/cm^2 which is ~3% higher than that of a thermal oxide layer [13,14]. Due to the high atomic density, the band discontinuity energy at the SiO_2/Si interface is high [13,14], leading to a decrease in the tunnelling probability of charge carriers through SiO_2.

Figure 4 shows the threshold voltage of the fabricated TFTs with the ultra-thin NAOS SiO_2/~20 nm CVD SiO_2 stack dielectric structure. The gate width was 10 μm, and the source-drain voltage was 0.1 V. The threshold voltages for the P-ch and N-ch TFTs were –0.5 and 0.5 V, respectively, almost independent of the gate length, i.e., with no short channel effect [17]. The low threshold voltages for both the P-ch and N-ch TFTs could be achieved because of a low oxide fixed charge density and a low interface state density.

Figure 5 shows the drain current vs. the source-drain voltage (I_d-V_{s-d}) curves for the fabricated TFTs with the ultra-thin NAOS SiO_2/~20 nm CVD SiO_2 stack dielectric structure. The gate length and width were 0.9 and 10 μm, respectively. The I_s-V_{s-d} curves showed a saturation characteristic with a high current even at the driving voltage of 2 V, indicating that both the P-ch and N-ch TFTs could be operated at 2 V. The consumed power by TFT, P, is approximately proportional to the square of the operation voltage, V [18]:

$$V = fCV^2 \tag{1}$$

where f is the signal frequency, and C is the charging and discharging equivalent capacitance.

Therefore, the present result demonstrates that the consumed power of the present TFTs is only 1/36 of that of the commercial TFTs operated at 12 V.

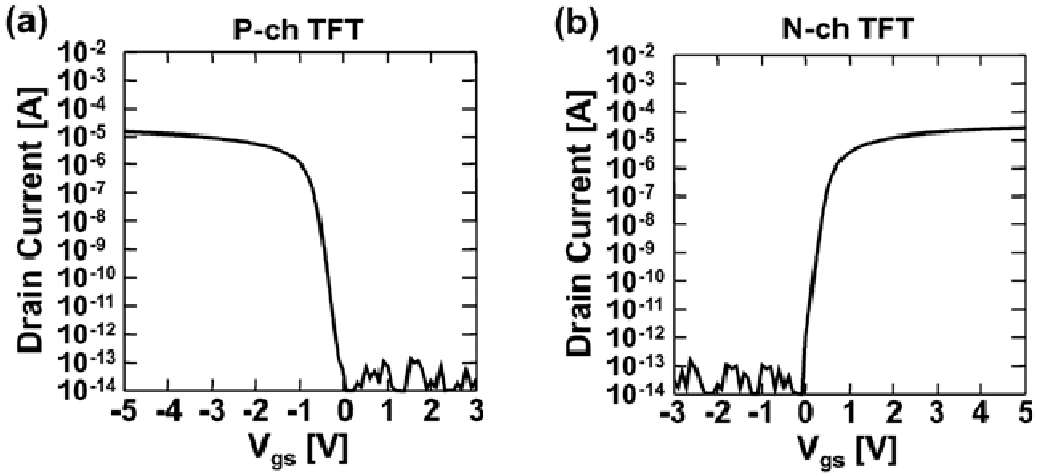

Fig. 6: *I_s-V_g curves for the P-ch and N-ch TFTs with the ultra-thin NAOS SiO_2/~20 nm CVD SiO_2 stack gate dielectric structure.*

Figure 6 shows the drain current vs. the gate voltage (I_d-V_g) curves for the fabricated TFTs. The gate length and width were 3.6, and 10 μm, respectively. The source-drain voltage was set at 0.1 V. The drain current rapidly increased with the gate voltage, and the sub-threshold swing for both the P-ch and N-ch TFTs was estimated to be ~80 mV/dec. The low sub-threshold swing close to the theoretical limit of 60 mV/dec. (i.e., $kT\ln 10/e$) at room temperature was due to the thin gate oxide and a low interface state density. The ratio between the on-current and the off-current, i.e., on/off ratio, was 10^9 for both the P-ch and N-ch TFTs. This on/off ratio was one or two orders of magnitude higher than those for conventional TFTs. The high on/off ratio is attributable to the low off-current within the noise level. The extremely low off-current demonstrates that a gate leakage current is effectively blocked by the ultra-thin NAOS SiO_2 layer.

5. Conclusion

We have fabricated TFTs with the ultra-thin NAOS SiO_2/~20 nm CVD SiO_2 stack gate dielectric structure. The fabricated TFTs possess low threshold voltages, i.e., –0.5 V for the P-ch TFTs and 0.5 V for the N-ch TFTs, and these TFTs can be operated at 2 V. Due to the low gate leakage current, the on-off ratio is 10^9, which is one or two orders of magnitude higher than those for conventional TFTs. The sub-threshold swing is ~80 mV/dec. due to the thin gate oxide layer and the low interface state density. These excellent TFT characteristics

are attributable to good electrical characteristics of the ultrathin NAOS SiO_2 layer such as the low leakage current density and the low interface state density.

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